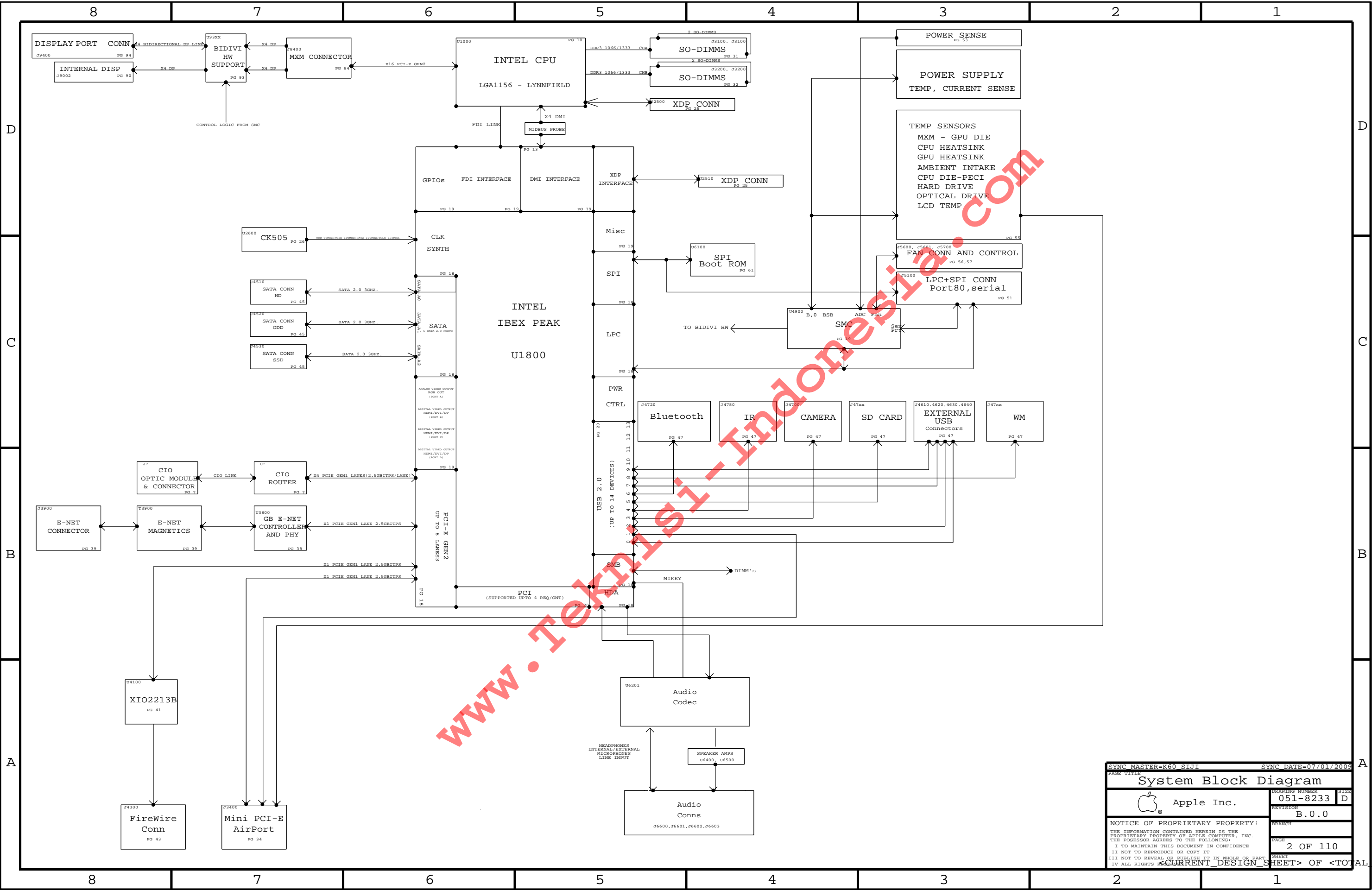



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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.						REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.						B	0000803841	PRODUCTION RELEASED	2009-10-09
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.									
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0439	PCBA,MLB,K23F,2.66GHZ	K23F,2P66GHZ_CPU,BASIC,CPUPOC_IMAX_100_120
639-0440	PCBA,MLB,K23F,2.80GHZ	K23F,2P80GHZ_CPU,BASIC,CPUPOC_IMAX_100_120
085-1023	PCBA,MLB,DEV,K23F	DEVELOPMENT_DEV_GROUP

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,XDP,BETTER,MXM,XDP_CPU_BPM,INT_VREF,PCH_VRM,BUF_CLK,PRODUCTION
DEV_GROUP	XDP_CONN,LPCPLUS,MOJOMUX,CPU_TDIODE,MEM_RESET_HW

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S8823	1	IC,ISEX PEAK B3,DESKTOP,FCBGA,PCH.P425	U1800	CRITICAL	
359S0157	1	IC,SLG2AP108,CLK GEN,CK505,QFN3	U2600	CRITICAL	BUF_CLK
341T0211	1	IC,EPI BOOTROM,K23F	U6100	CRITICAL	
338S0765	1	IC,XIO2211ZAY,1394B_PCIE,PHY/SINK	U4100	CRITICAL	
343S0485	1	IC,BCM5764M,68PIN QFN	U3700	CRITICAL	
341T0213	1	IC,FLASH,45DB0011D,SOIC-8S1	U3701	CRITICAL	
511S0063	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3810	1	LFD,SILLC,FHQ,2.66,95W,1333,B1,8M,LGR	CPU	CRITICAL	2P66GHZ_CPU
337S3811	1	LFD,SLBN7,FHQ,2.80,95W,1333,B1,8M,LGR	CPU	CRITICAL	2P80GHZ_CPU

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

K23F PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8233	1	SCH,K23F,MLB	SCH1		K23F
820-2733	1	PCBF,K23F,MLB	MLB1		K23F
(338S0489 - BLNK) 341T0212	1	IC,SMC,K23F	U4900	CRITICAL	K23F

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BOM Configuration

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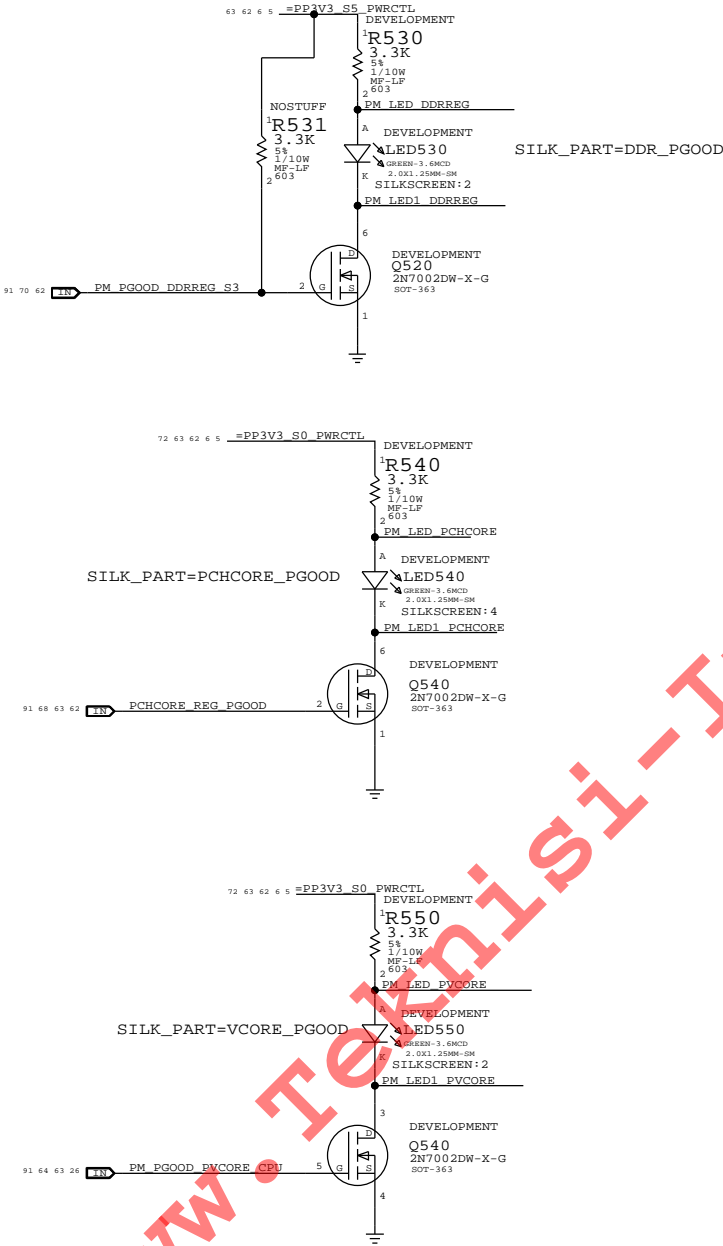
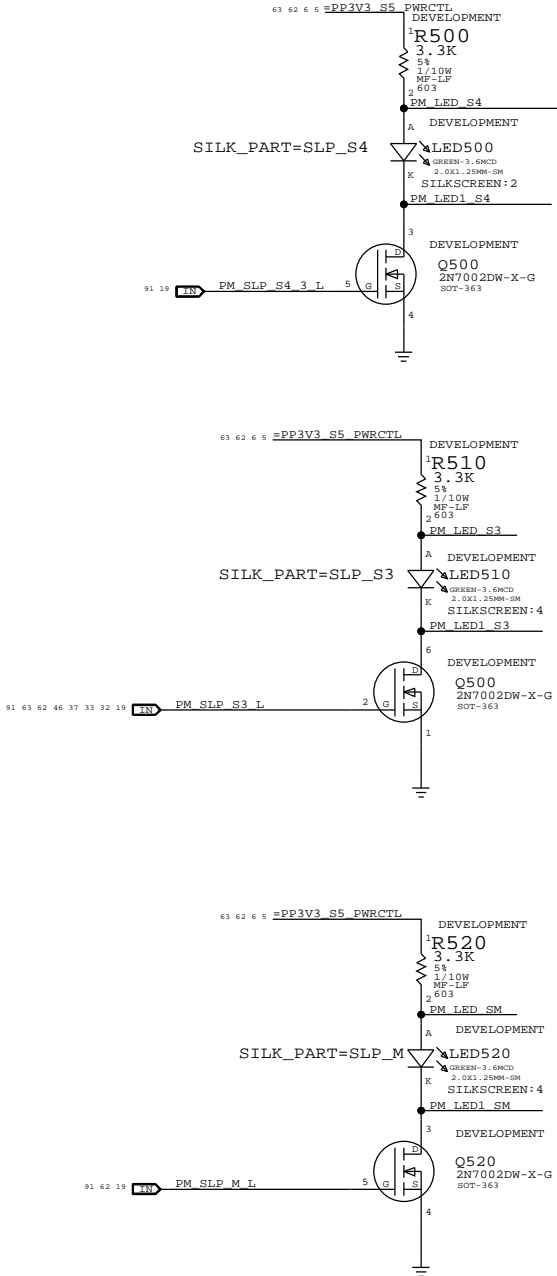
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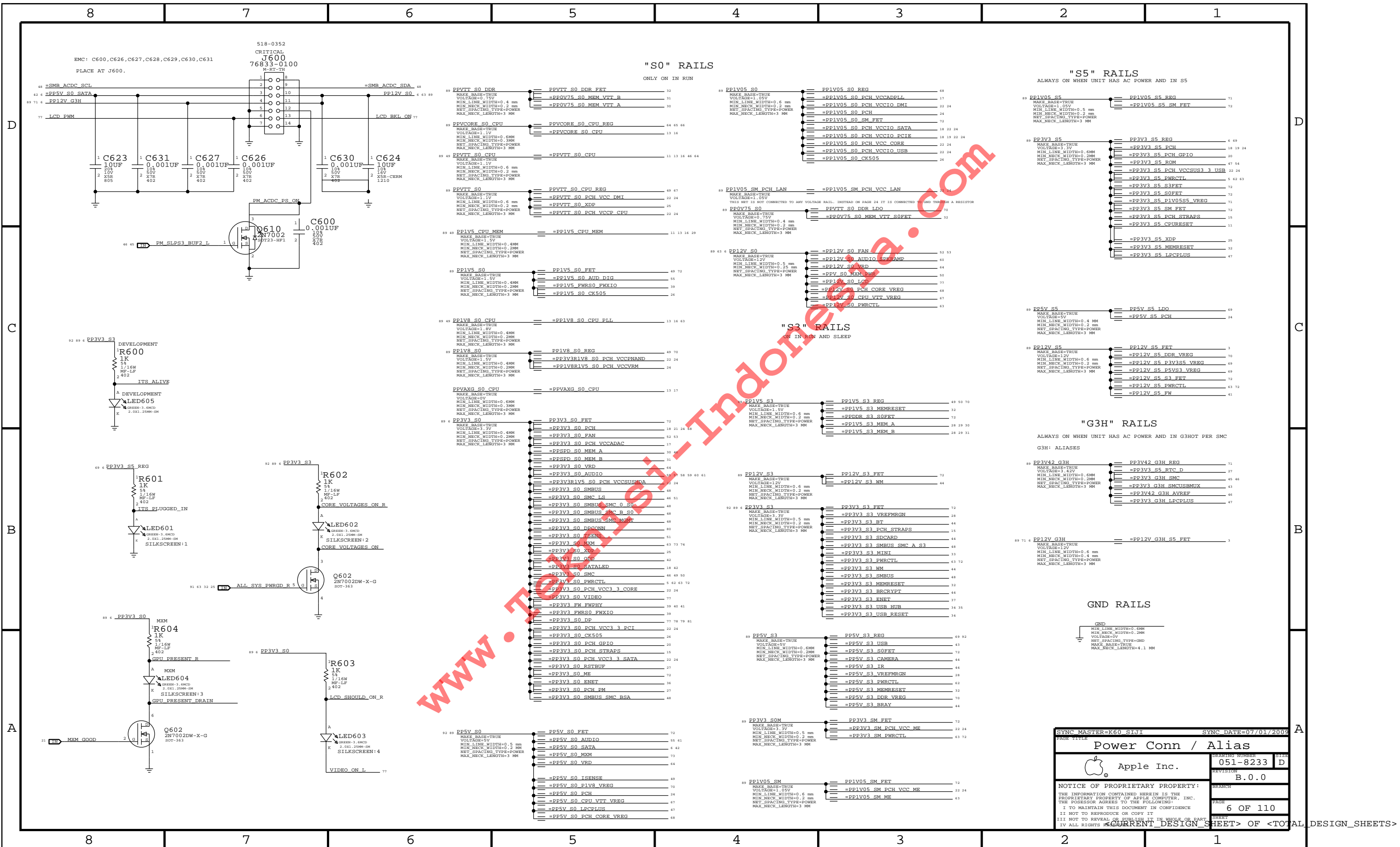
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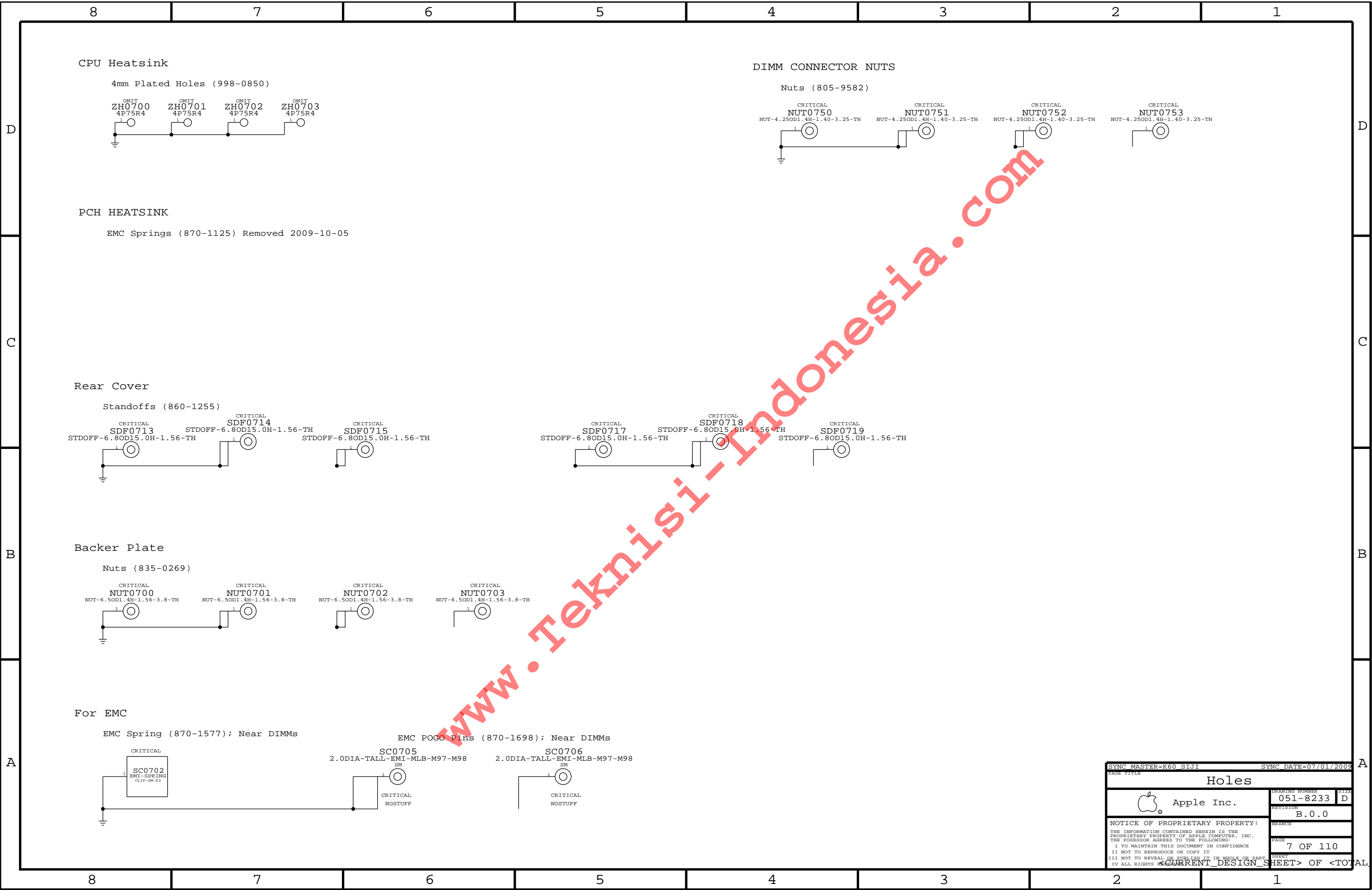



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

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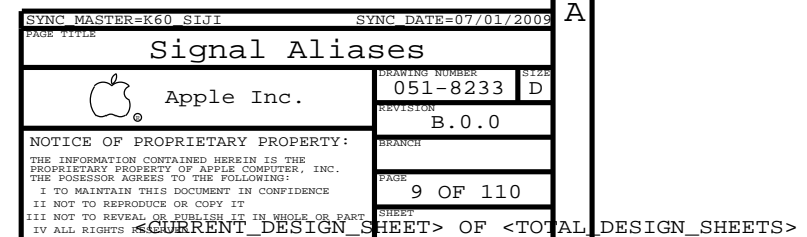
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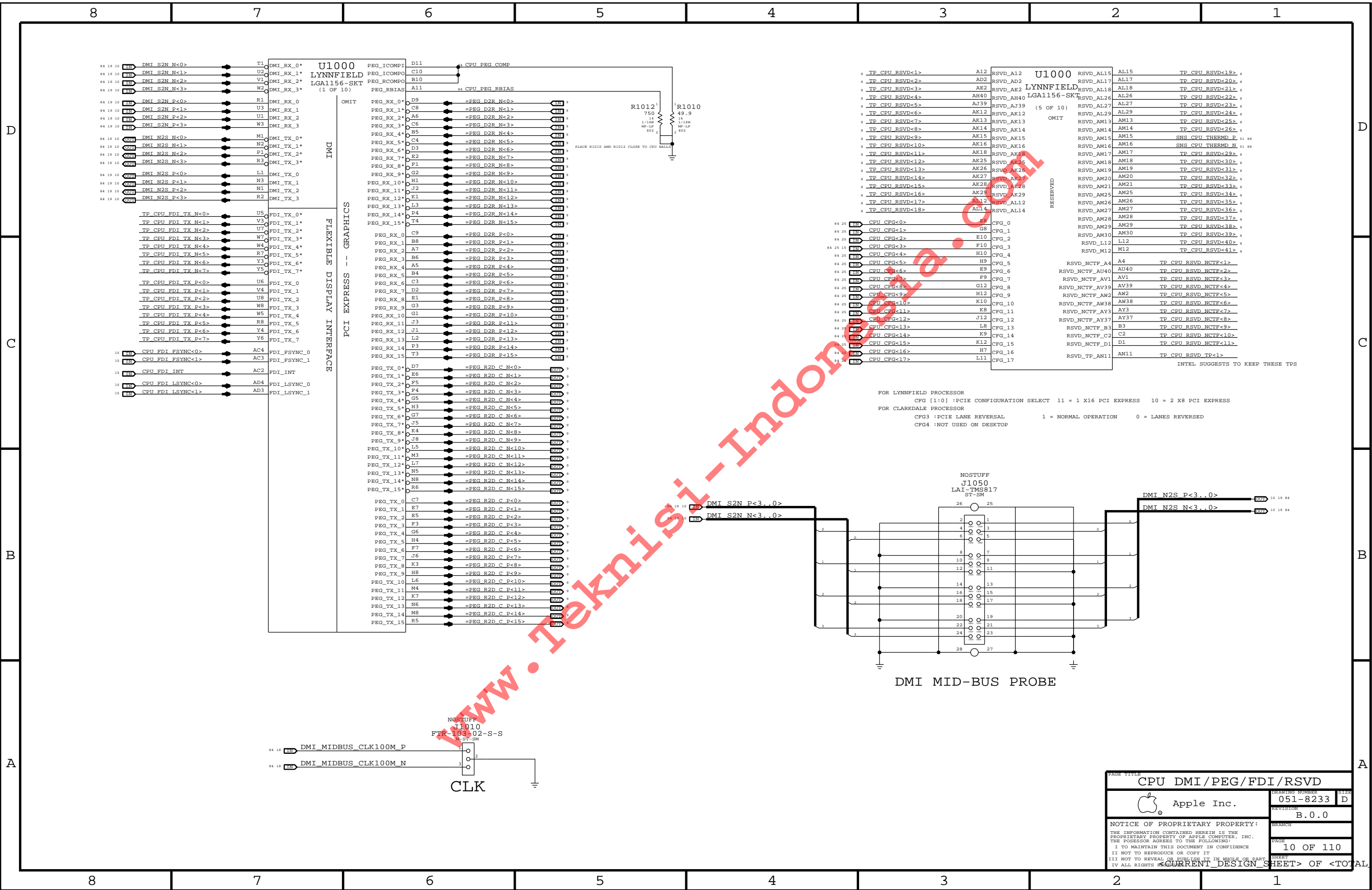


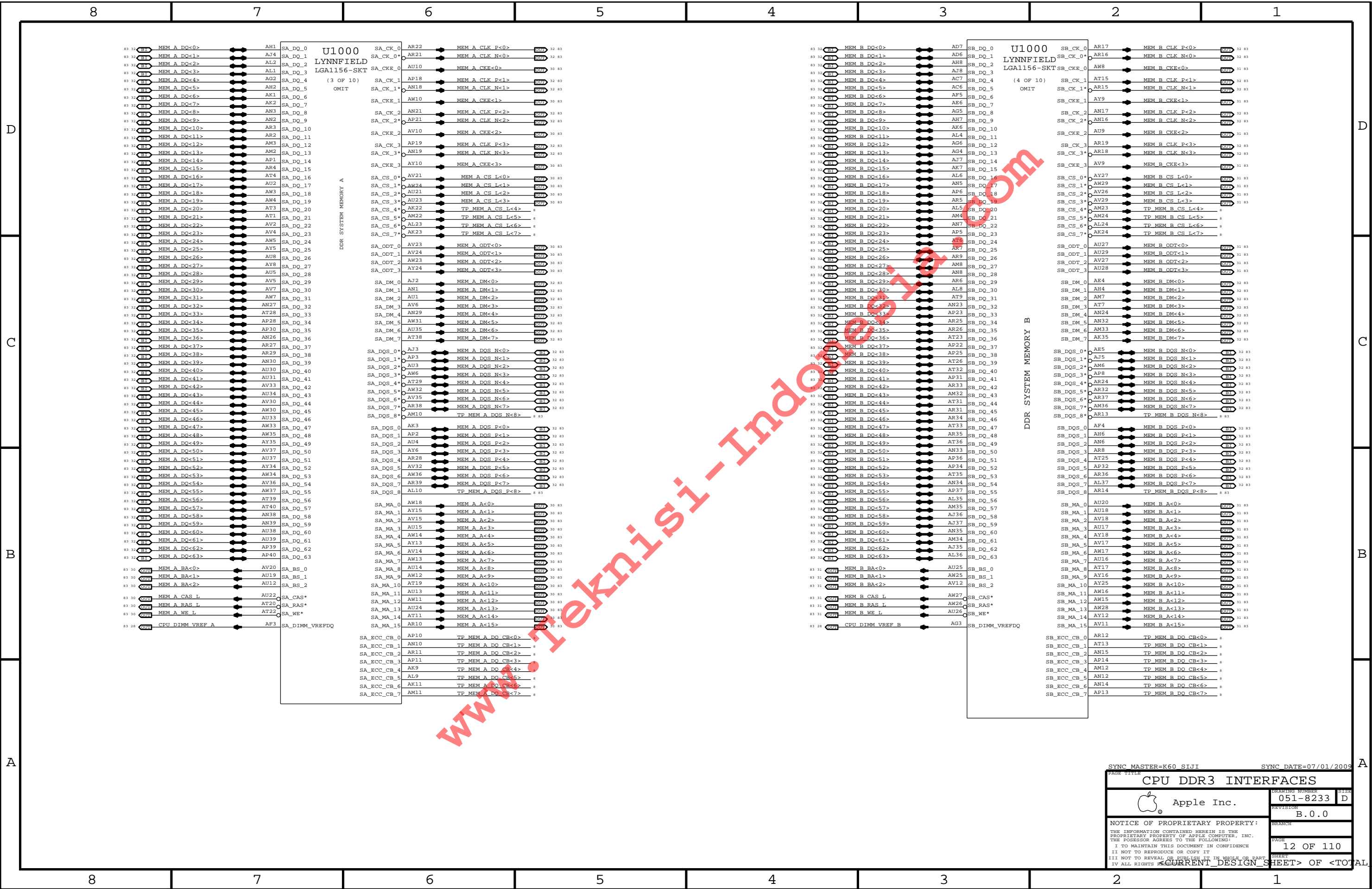


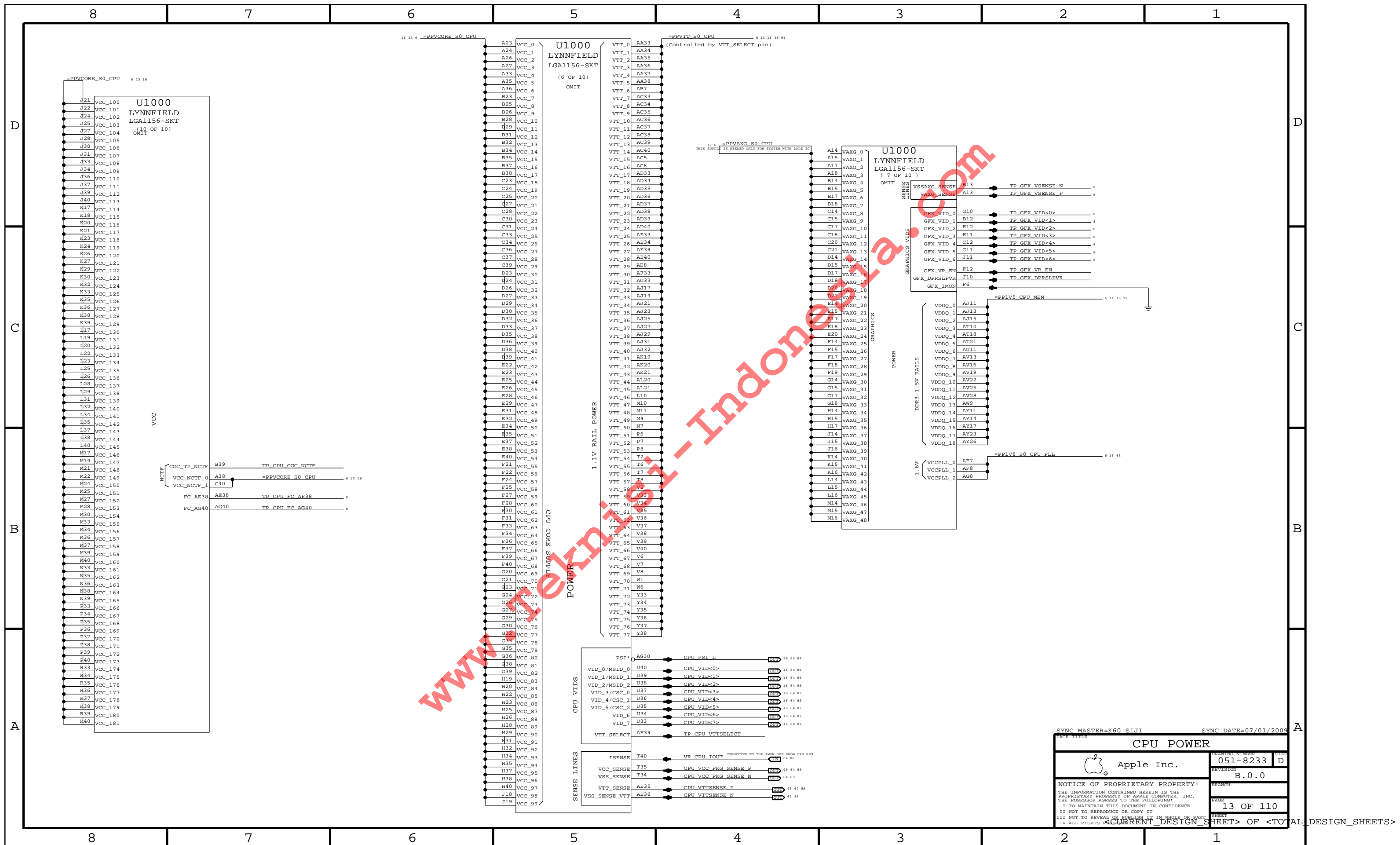
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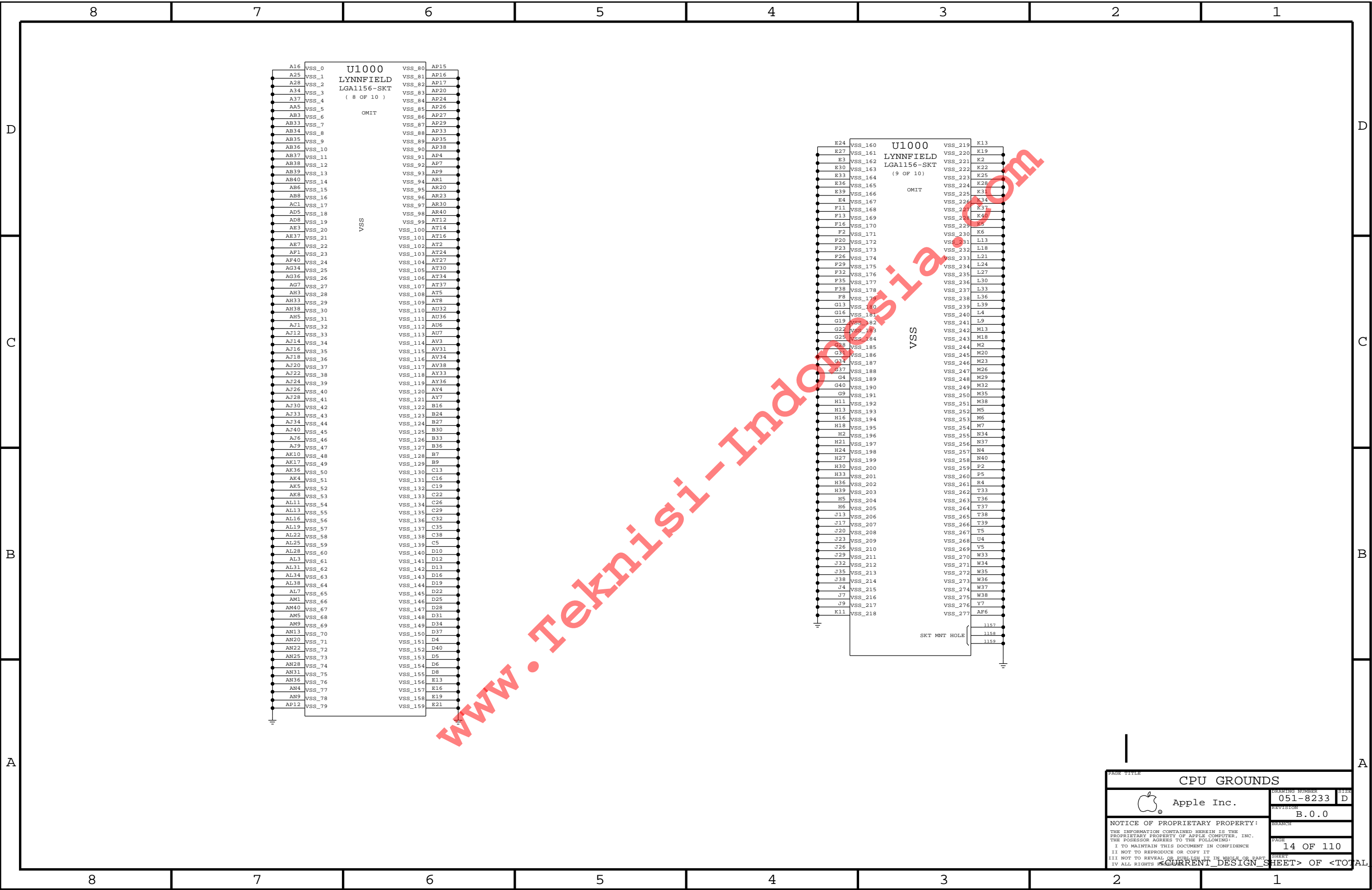
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NO_TEST=TRUE</p> <p>TP LPC DREQ0 L == NC LPC DREQ0 L MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>NC ON UNUSED NAND ALIASES</p> <p>TP NV CE L<3..0> == NC NV CE L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP NV DQS<1..0> == NC NV DQS<1..0> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP NV DQ<15..0> == NC NV DQ<15..0> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP NV RB L == NC NV RB L MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP NV WR RE L<1..0> == NC NV WR RE L<1..0> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP NV WE CK L<1..0> == NC NV WE CK L<1..0> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>NC ON UNUSED MISC ALIASES</p> <p>TP JTAG XDP TRST L == NC JTAG XDP TRST L MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP PCH PWM0 == NC PCH PWM0 MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP PCH PWM1 == NC PCH PWM1 MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP PCH PWM2 == NC PCH PWM2 MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP PCH PWM3 == NC PCH PWM3 MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP PCH SST == NC PCH SST MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>NC ON UNUSED MEM ALIASES</p> <p>TP MEM A CS L<7..4> == NC MEM A CS L<7..4> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP MEM A DQ CB<7..0> == NC MEM A DQ CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP MEM A DOS N<8> == NC MEM A DOS N<8> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP MEM A DOS P<8> == NC MEM A DOS P<8> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP MEM B CS L<7..4> == NC MEM B CS L<7..4> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP MEM B DQ CB<7..0> == NC MEM B DQ CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP MEM B DOS N<8> == NC MEM B DOS N<8> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP MEM B DOS P<8> == NC MEM B DOS P<8> MAKE_BASE=TRUE NO_TEST=TRUE</p>				<p>NC ON UNUSED SATA ALIASES</p> <p>TP SATA D D2RN == NC SATA D D2RN MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA D D2RP == NC SATA D D2RP MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA D R2D CN == NC SATA D R2D CN MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA D R2D CP == NC SATA D R2D CP MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA E D2RN == NC SATA E D2RN MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA E D2RP == NC SATA E D2RP MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA E R2D CN == NC SATA E R2D CN MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA E R2D CP == NC SATA E R2D CP MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA F D2RN == NC SATA F D2RN MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA F D2RP == NC SATA F D2RP MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA F R2D CN == NC SATA F R2D CN MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP SATA F R2D CP == NC SATA F R2D CP MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>NC ON UNUSED DISPLAY ALIASES</p> <p>TP CRT IG DDC CLK == NC CRT IG DDC CLK MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP CRT IG DDC DATA == NC CRT IG DDC DATA MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP CRT IG RED == NC CRT IG RED MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP CRT IG GREEN == NC CRT IG GREEN MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP CRT IG BLUE == NC CRT IG BLUE MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP CRT IG HSYNC == NC CRT IG HSYNC MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP CRT IG VSYNC == NC CRT IG VSYNC MAKE_BASE=TRUE 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N<3..0> == NC PCI T28 R2D C N<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP PCI T28 R2D C P<3..0> == NC PCI T28 R2D C P<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP HDA SDIN1 == NC HDA SDIN1 MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP HDA SDIN2 == NC HDA SDIN2 MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP HDA SDIN3 == NC HDA SDIN3 MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP PCIE CLK100M PE5P == NC PCIE CLK100M PE5P MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP PCIE CLK100M PE5N == NC PCIE CLK100M PE5N MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP NV RCOMP == NC NV RCOMP MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>PCIE CLK100M EXCARD P == NC PCIE CLK100M EXCARD P MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>PCIE CLK100M EXCARD N == NC PCIE CLK100M EXCARD N MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP USB 7N == NC USB 7N MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP USB 7P == NC USB 7P MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP USB 6N == NC USB 6N MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP USB 6P == NC USB 6P MAKE_BASE=TRUE NO_TEST=TRUE</p> <p>TP USB 1N == NC USB 1N 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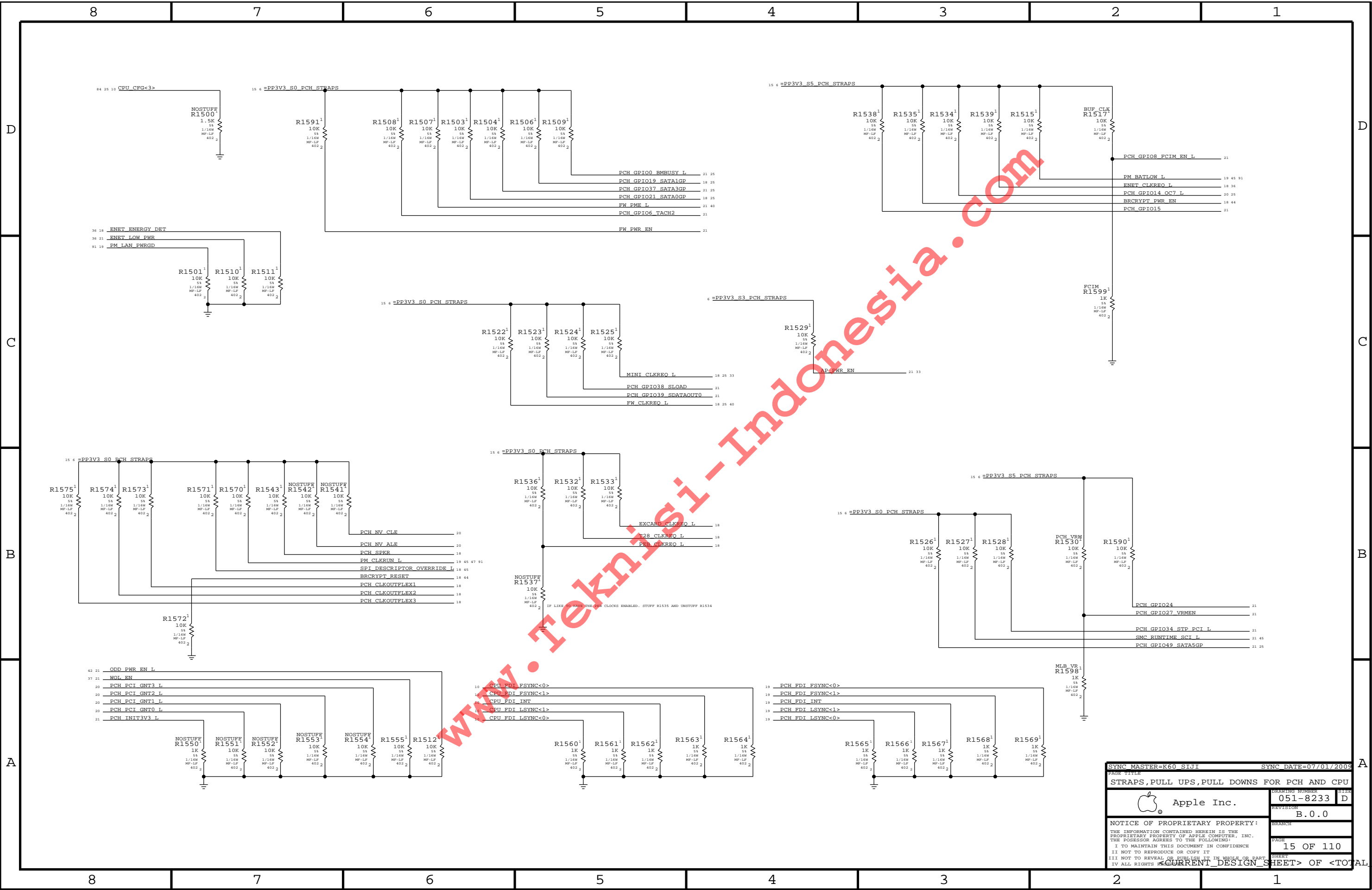




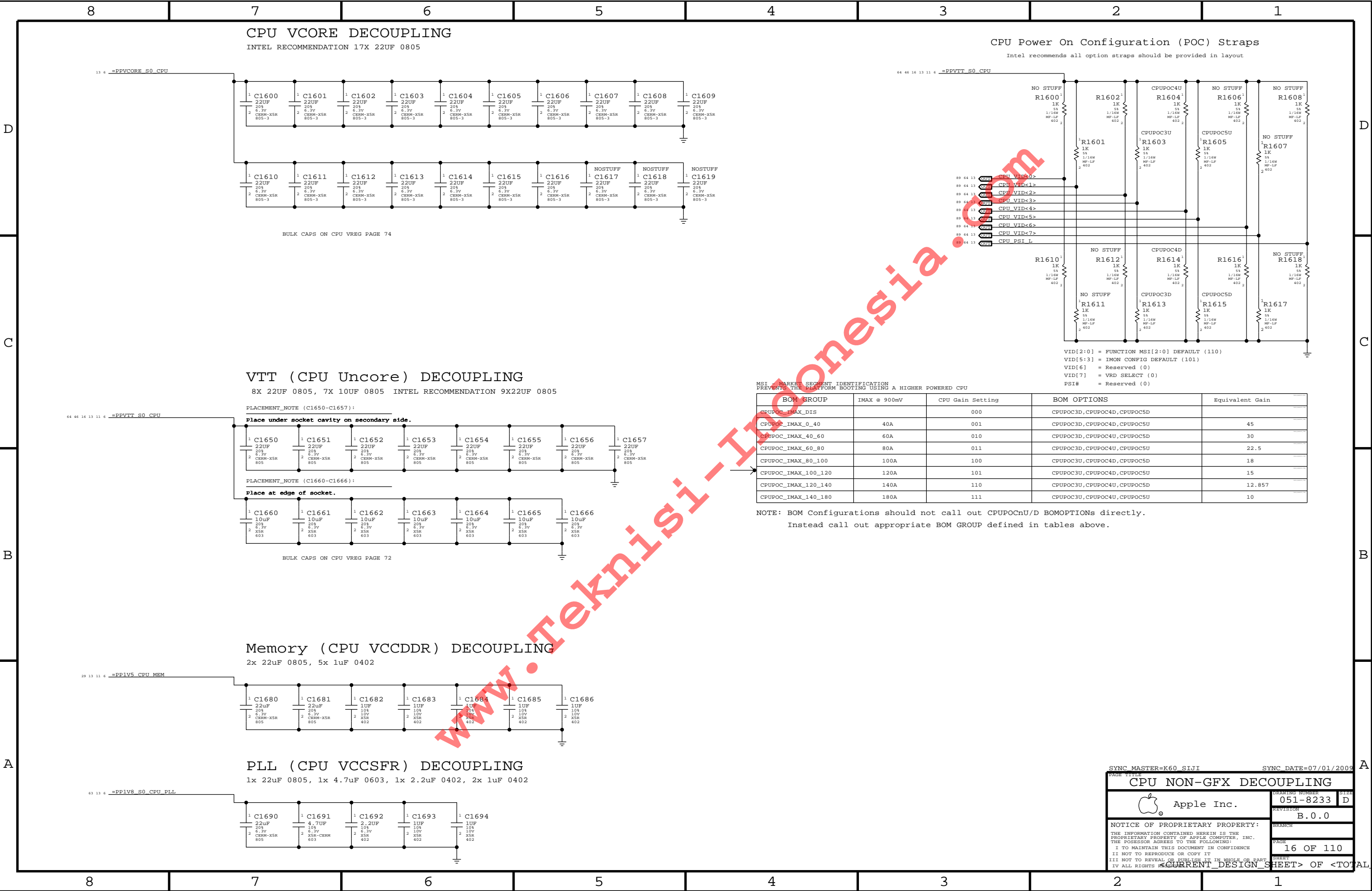


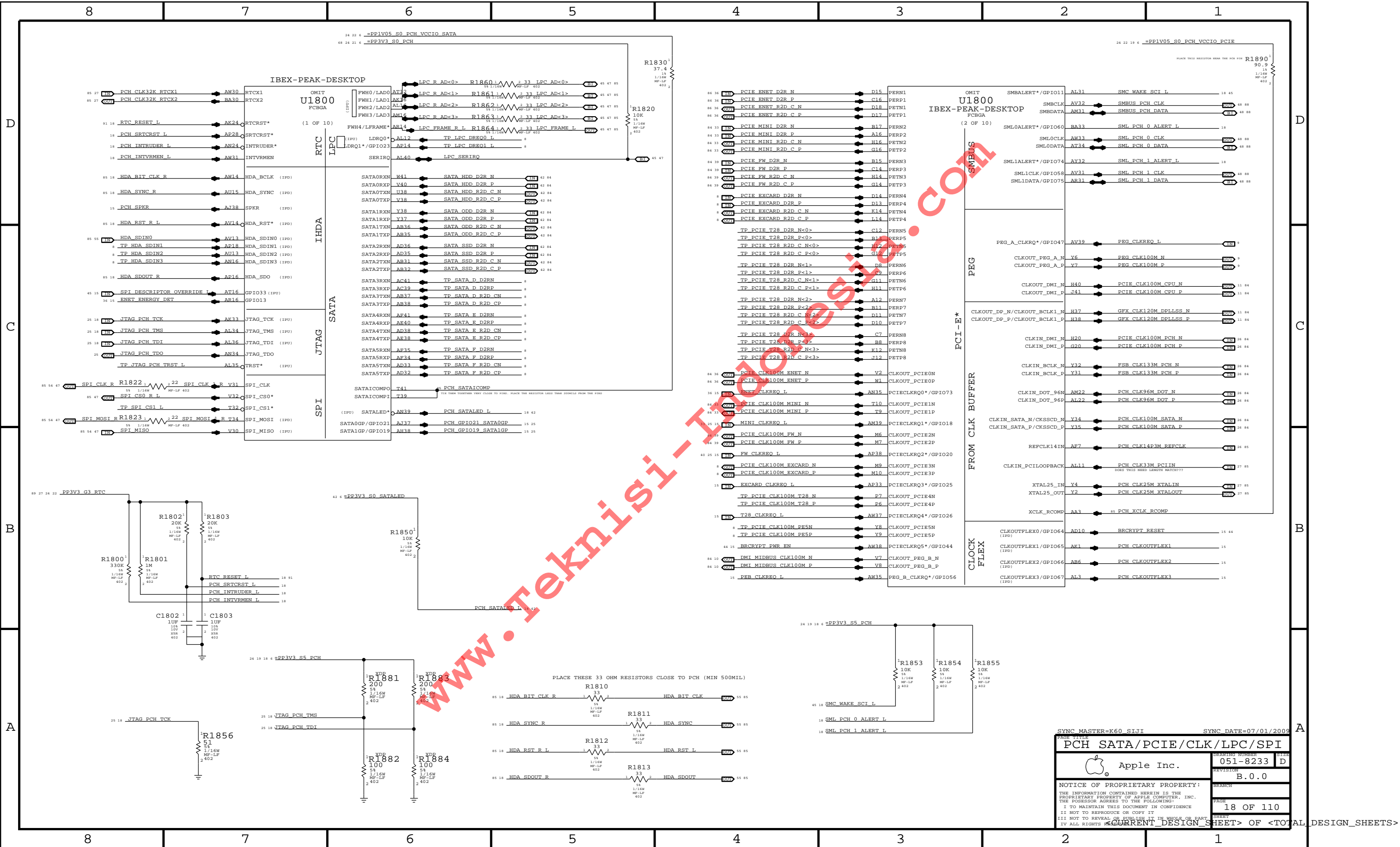


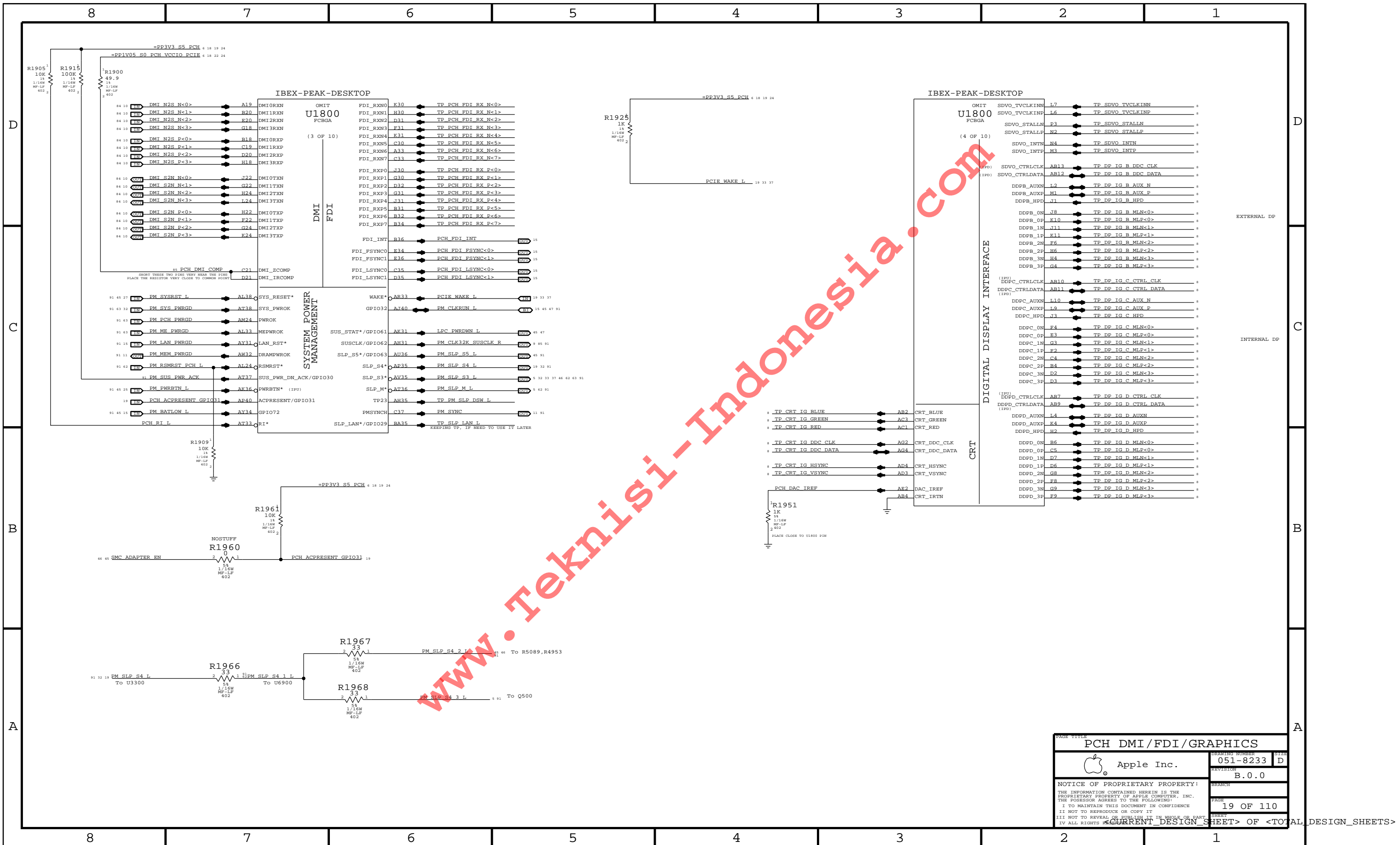


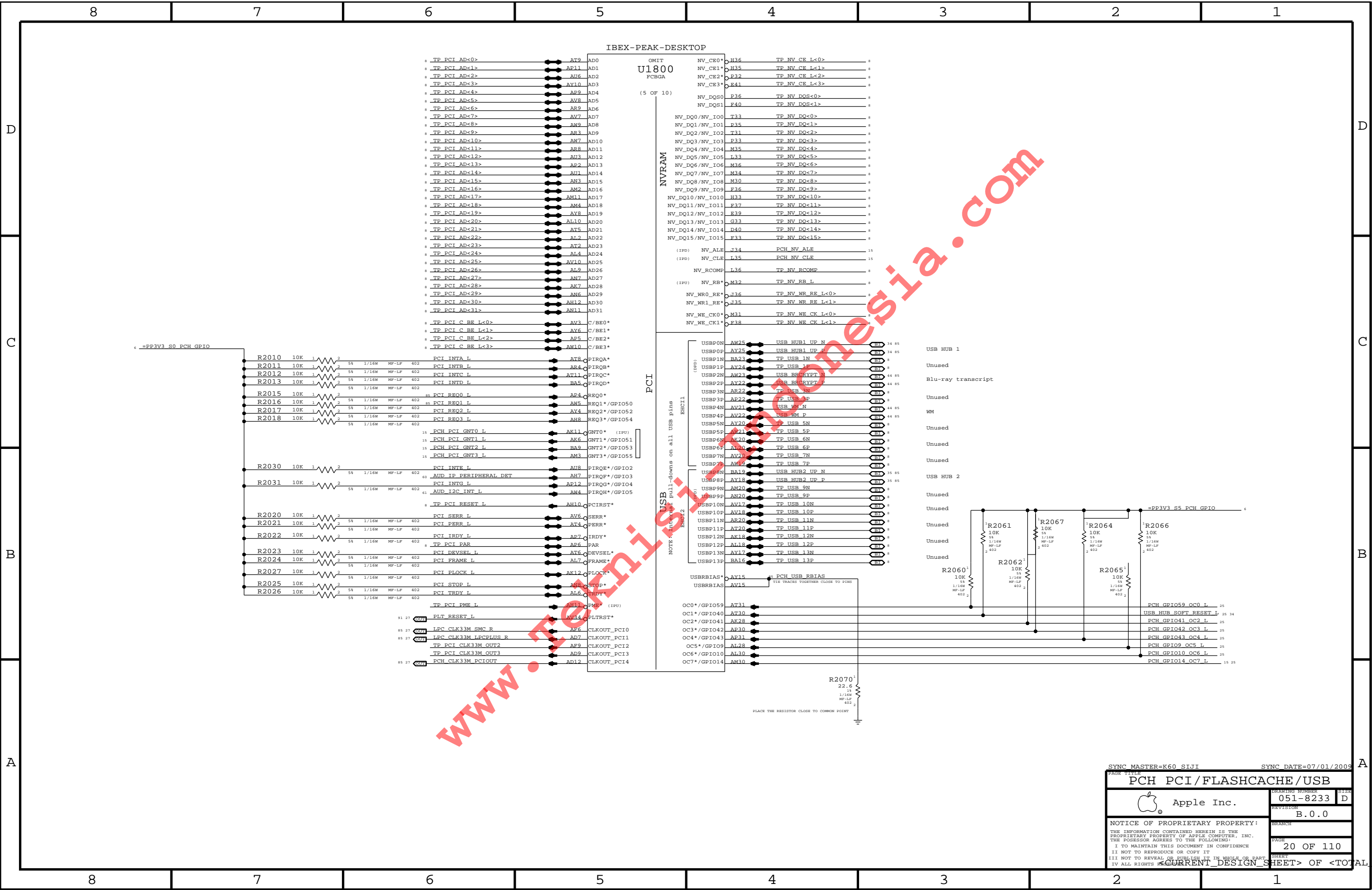


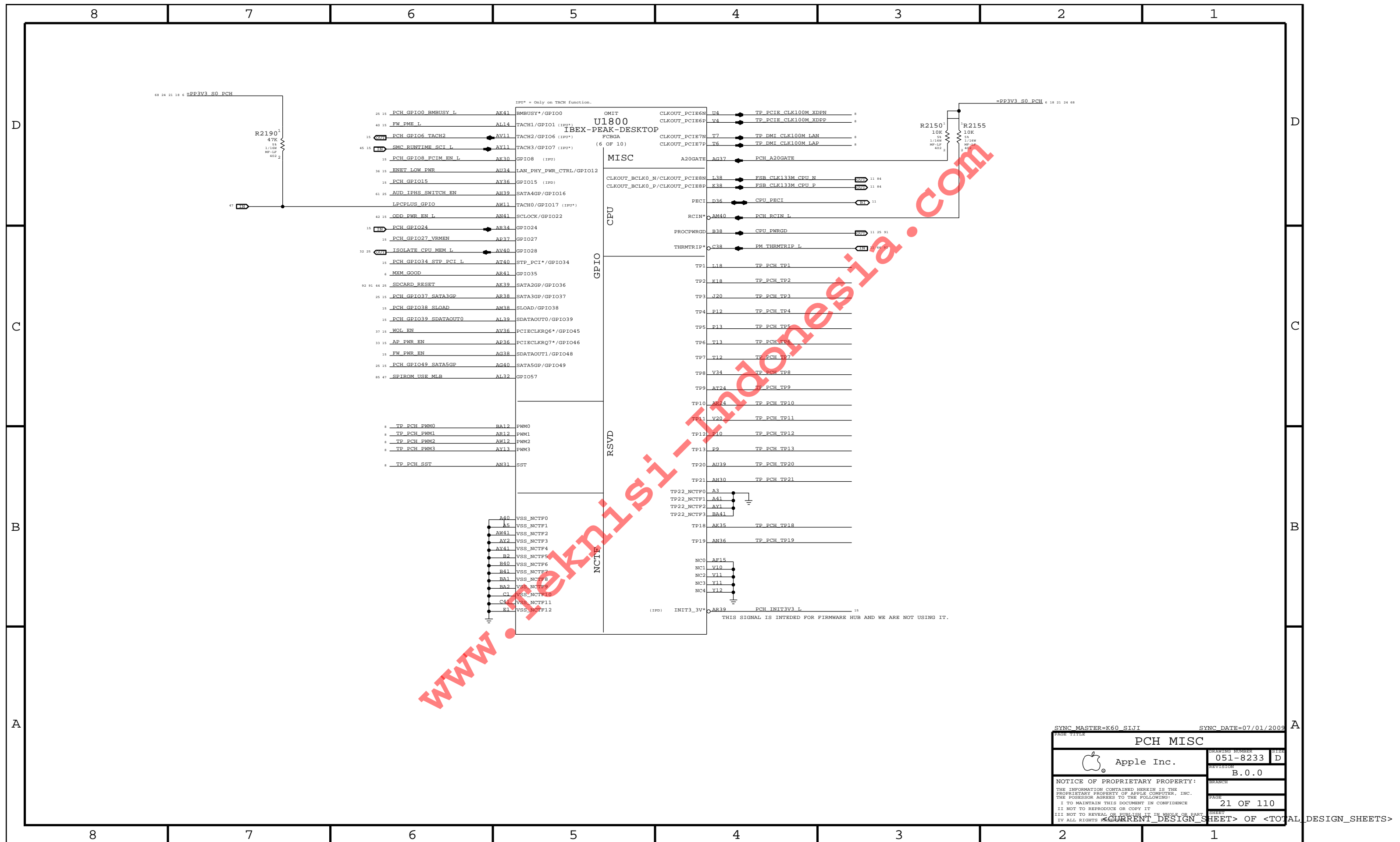
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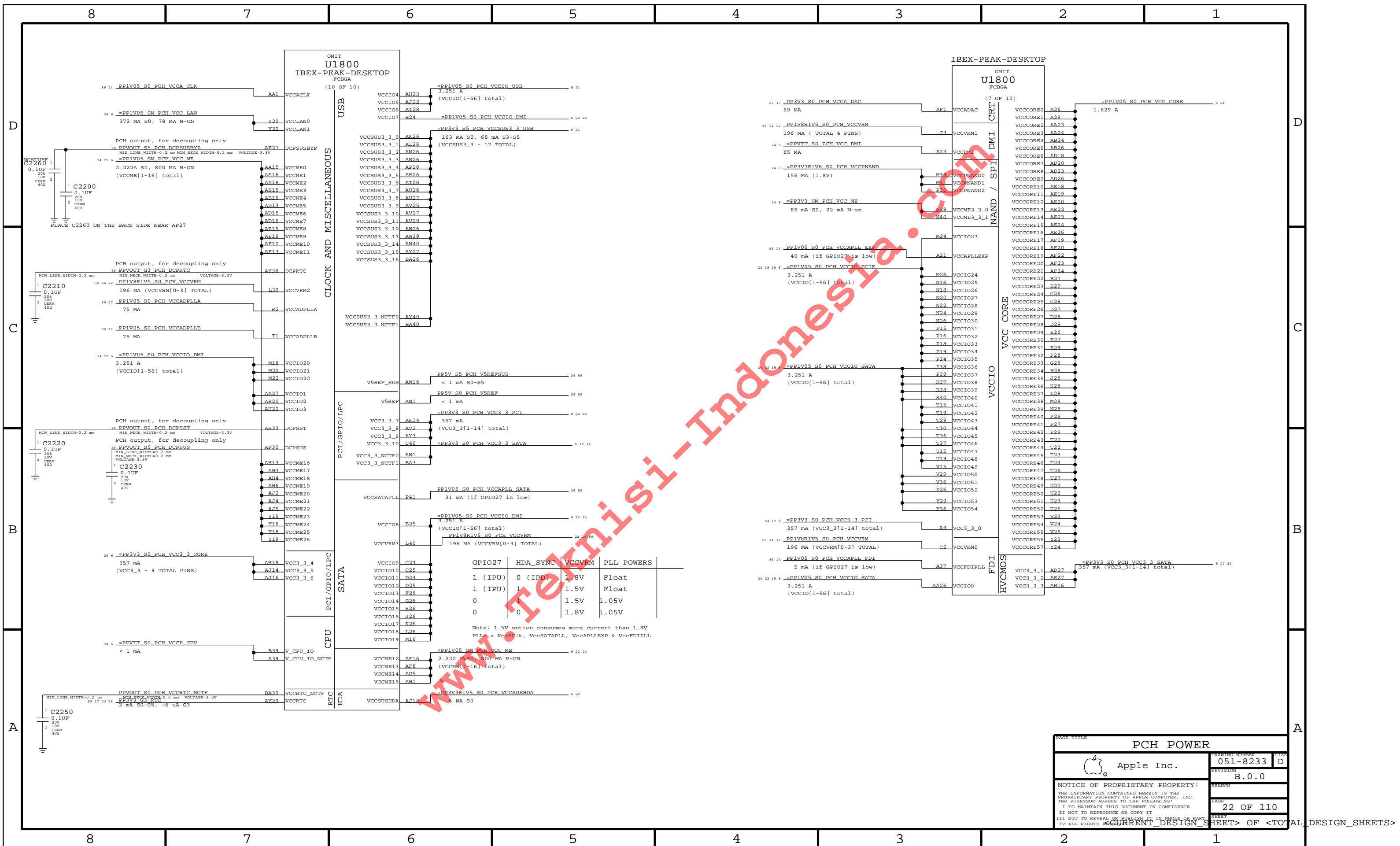


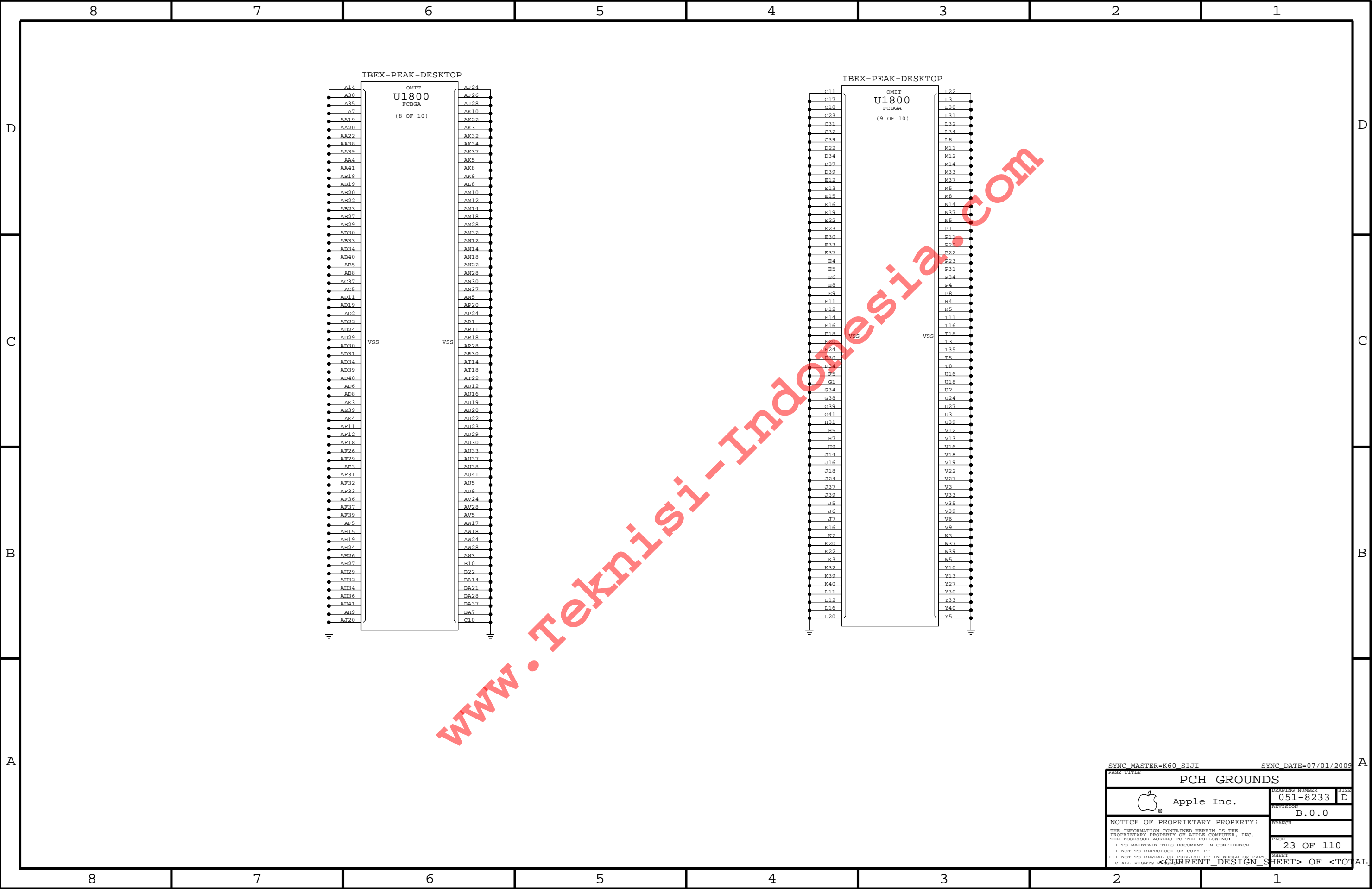


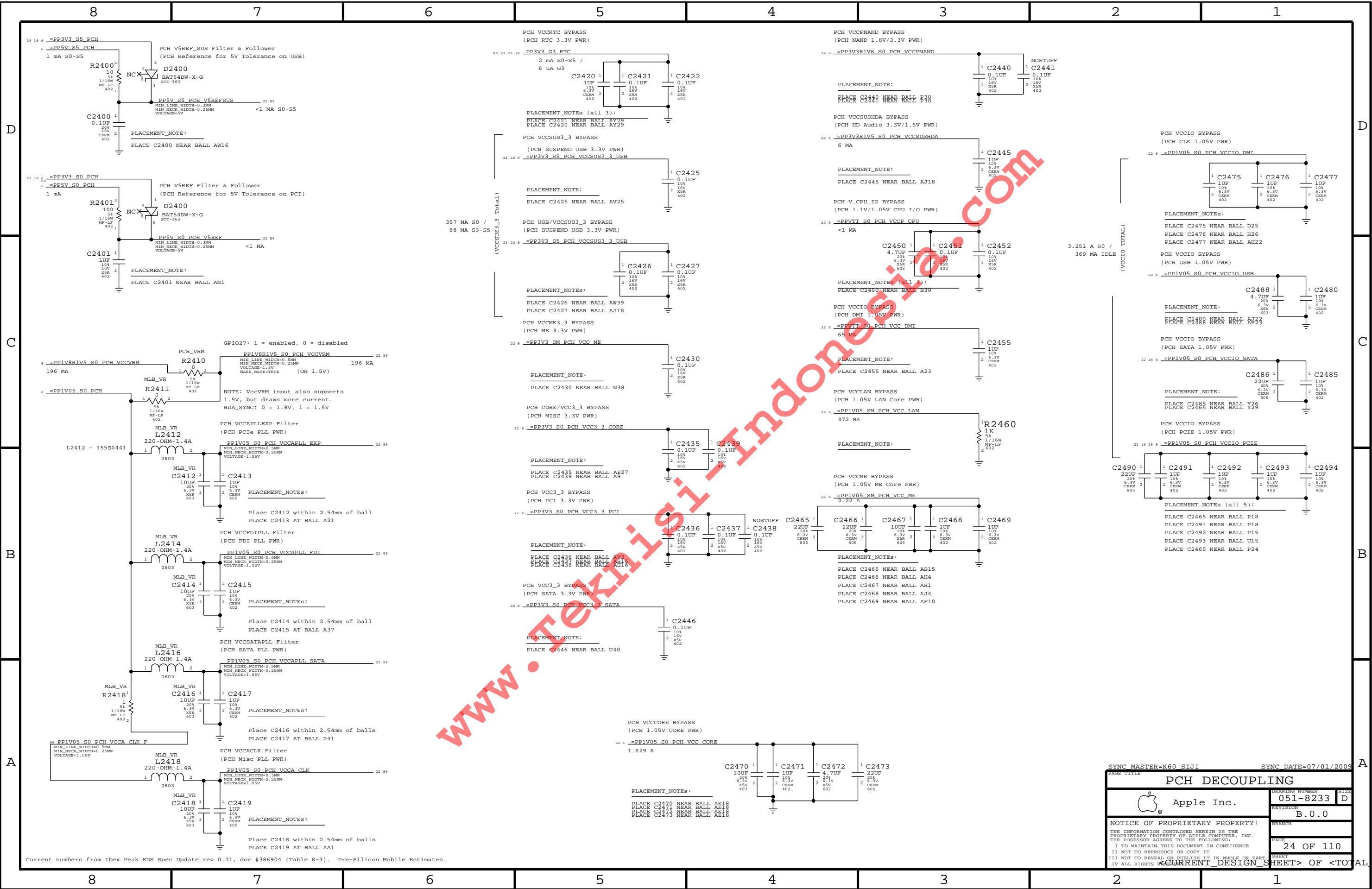













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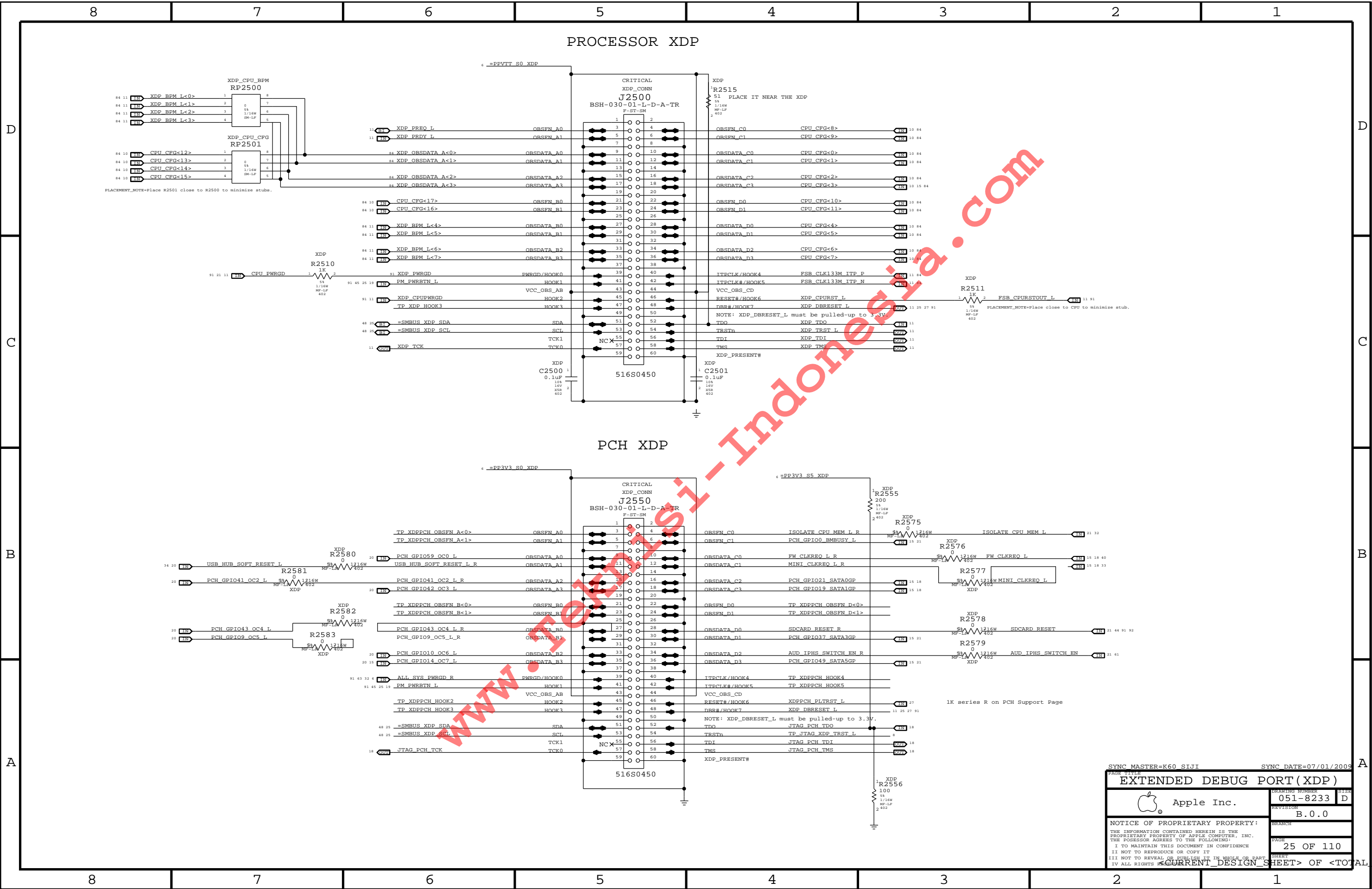
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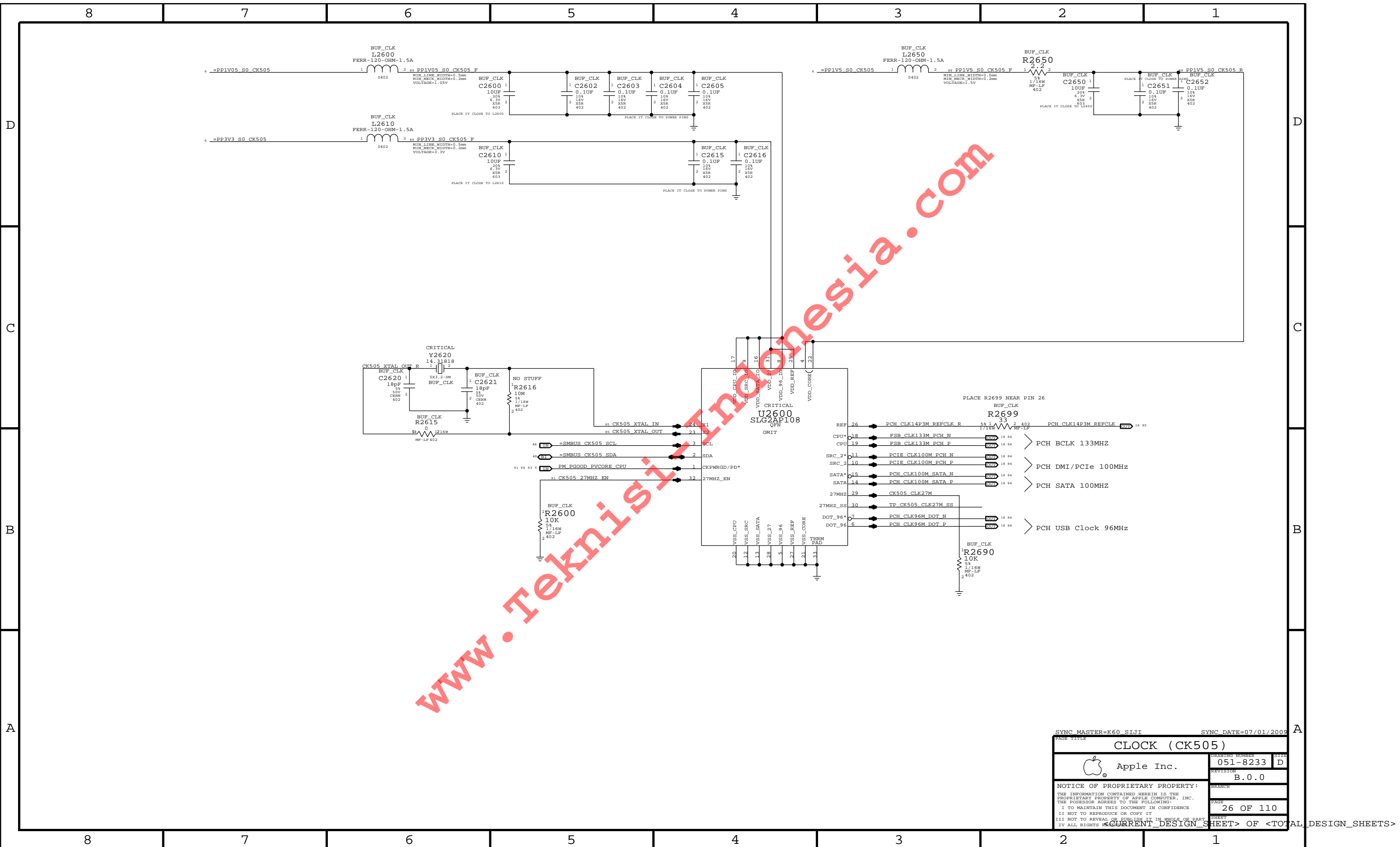
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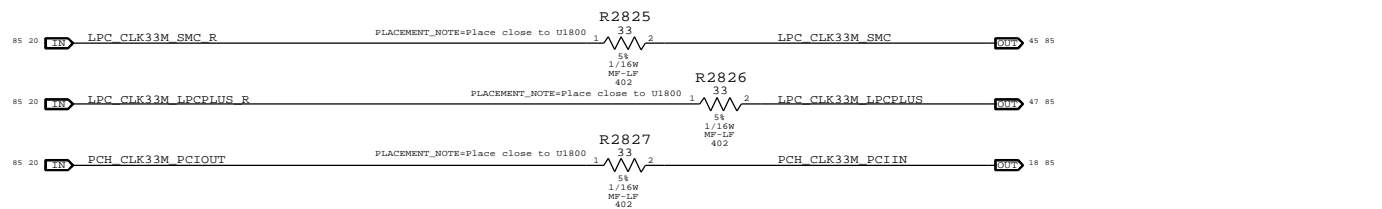
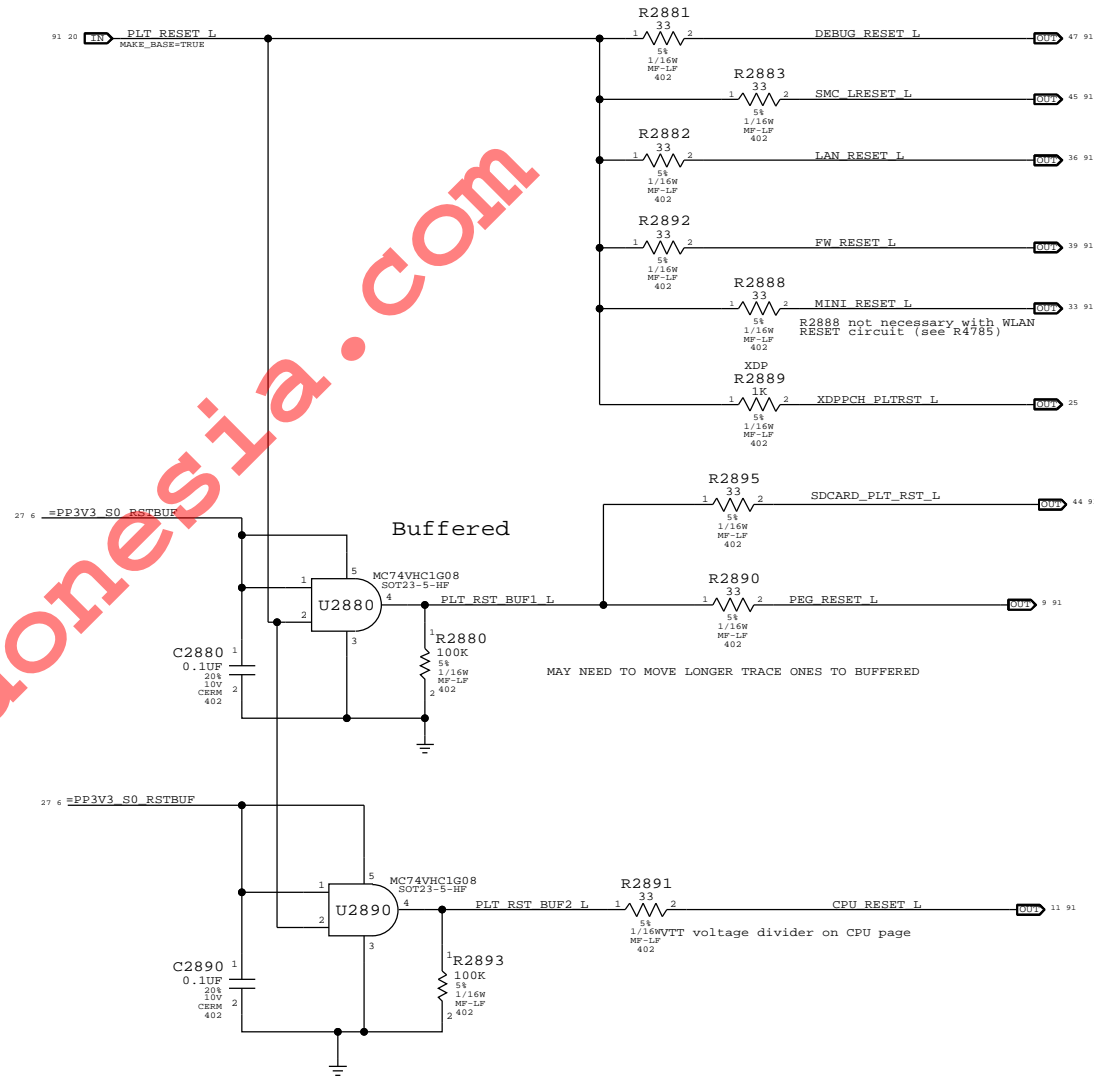
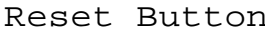
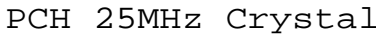
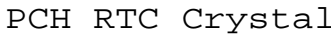
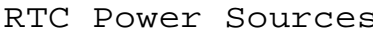
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SHEET

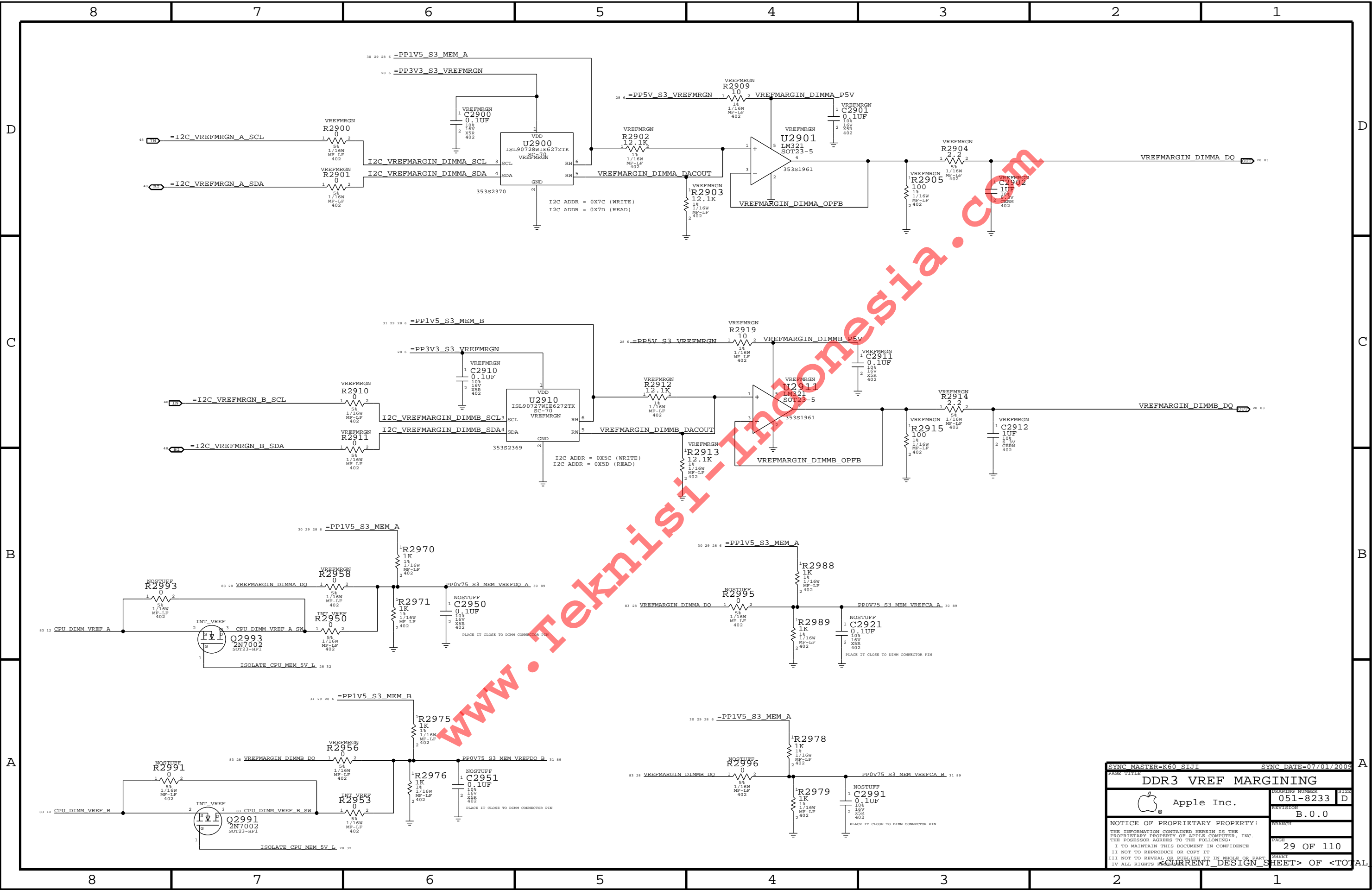
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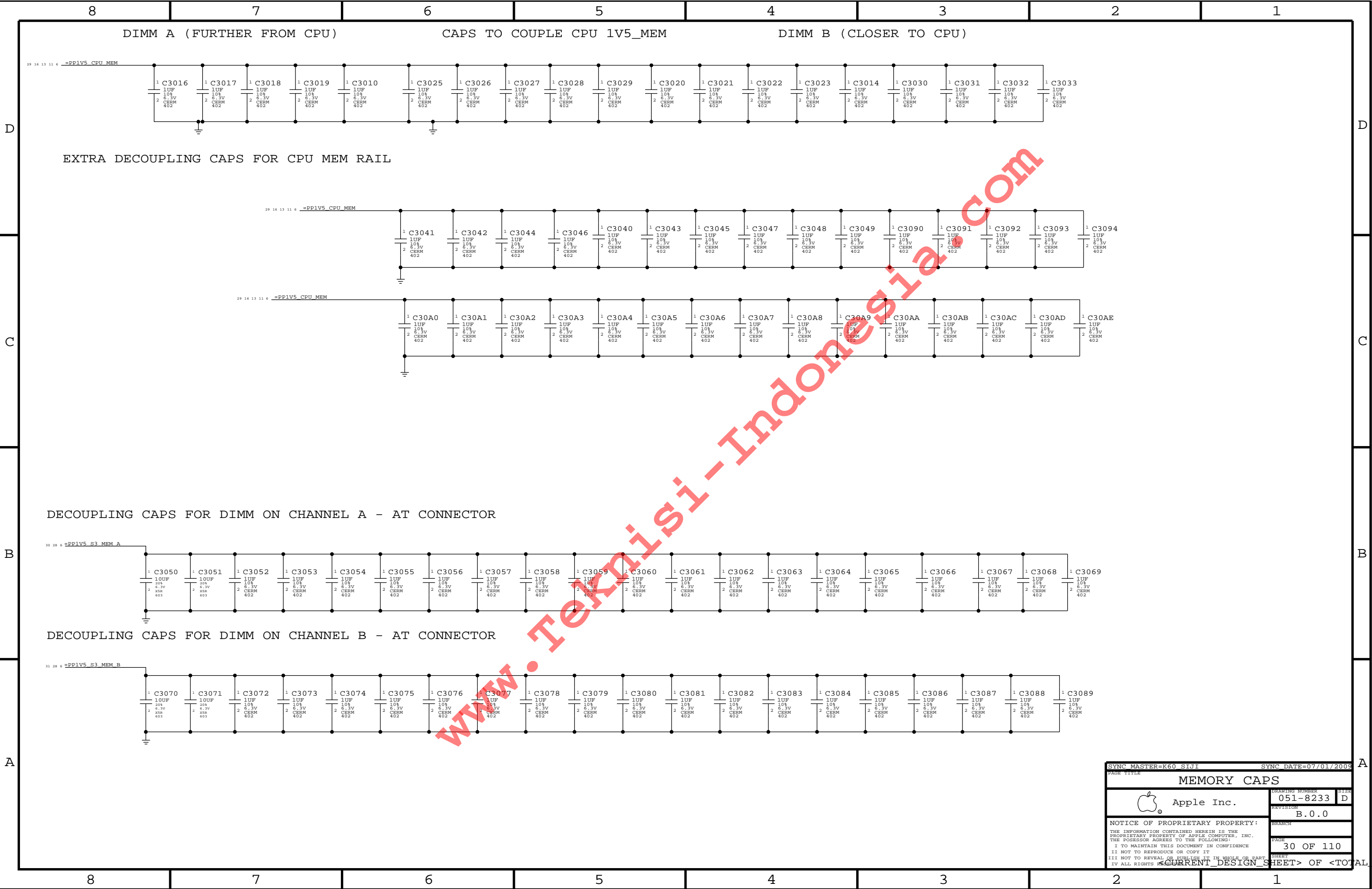


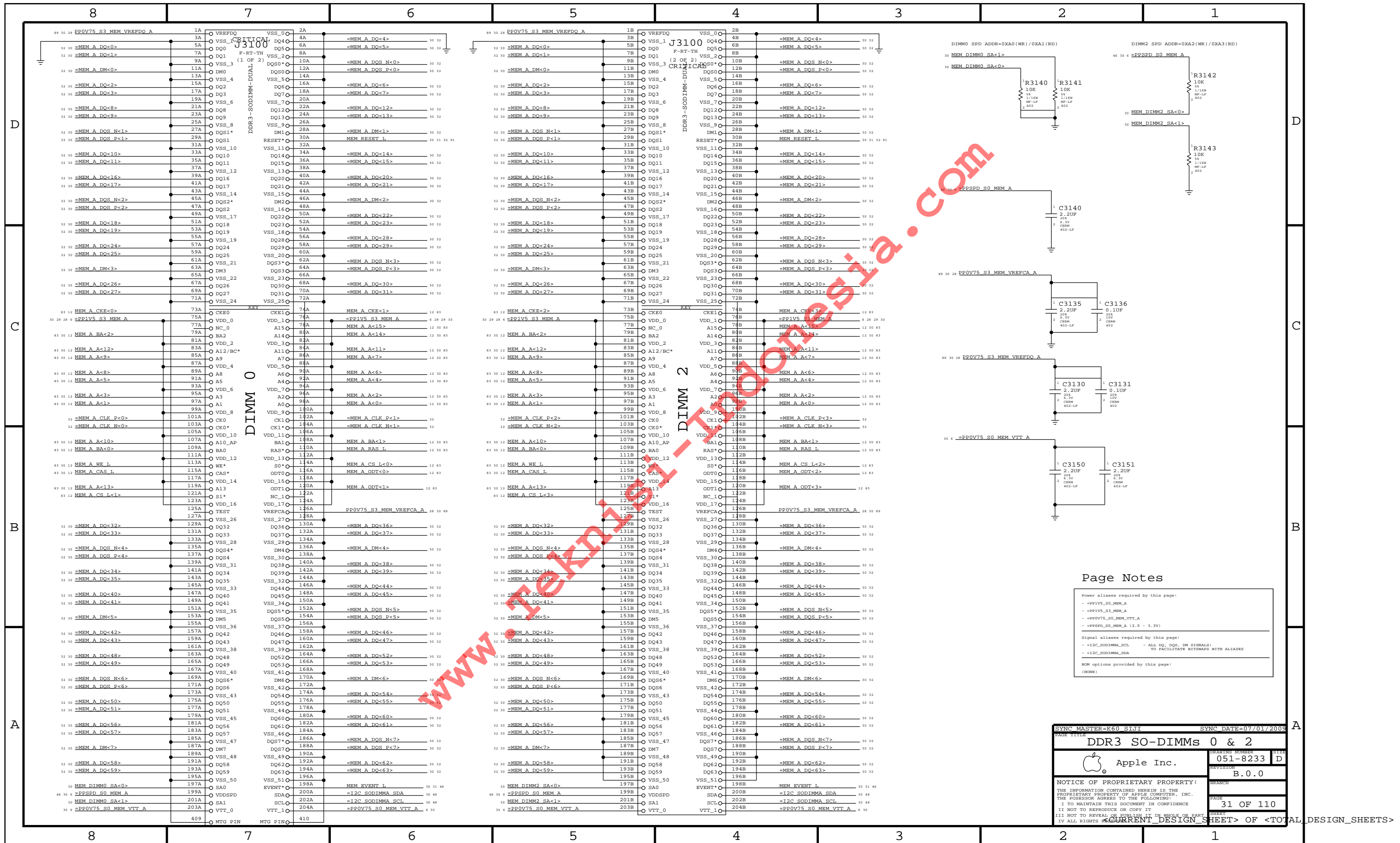


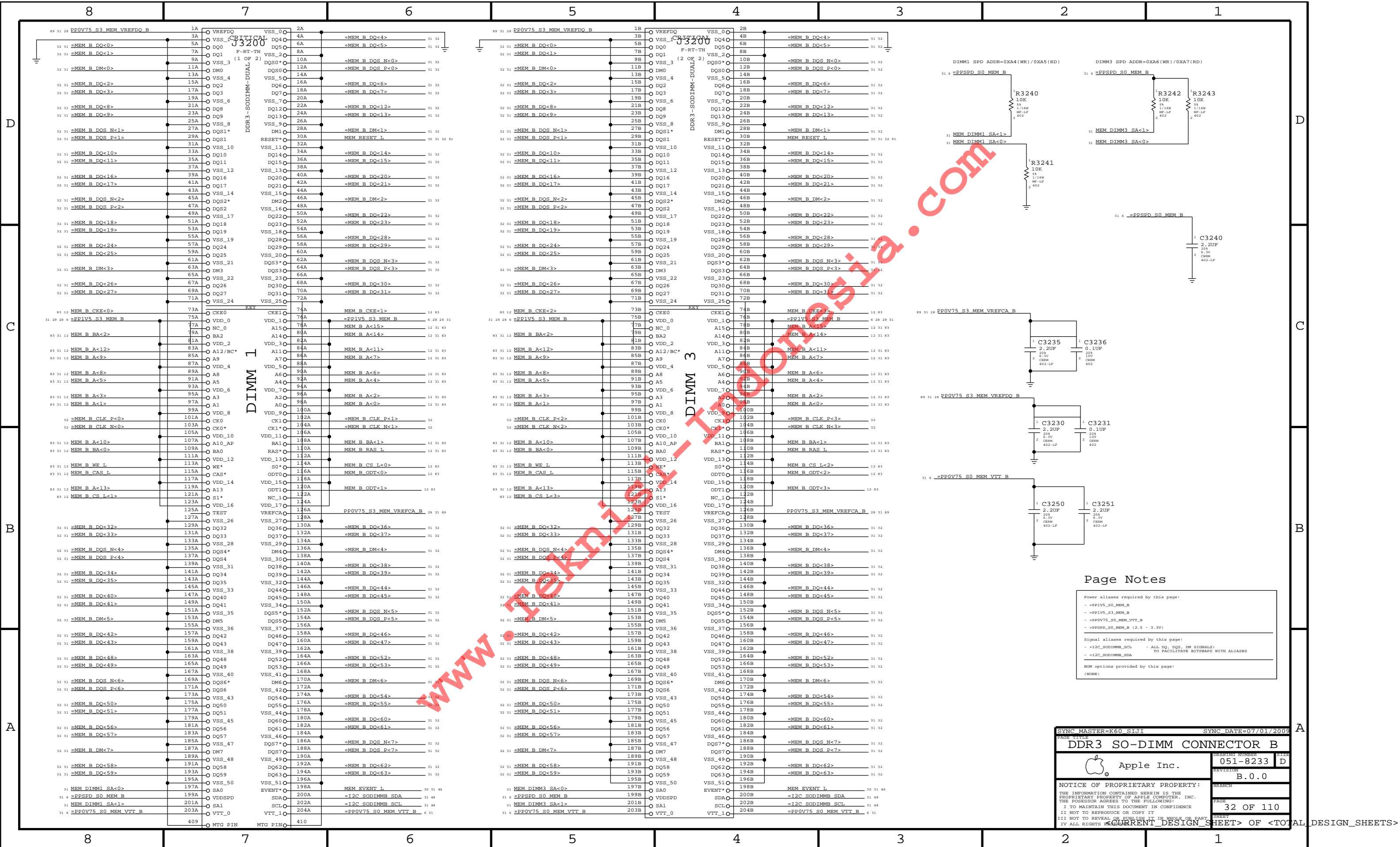
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Page Notes

- Power aliases required by this page:
- PP1V5_S0_MEM_B
 - PP1V5_S3_MEM_B
 - PP0V75_S0_MEM_VTT_B
 - PPSPD_S0_MEM_B (2.5 - 3.3V)
- Signal aliases required by this page:
- I2C_SODIMMB_SCL - ALL DQ, DQS, DM SIGNALS TO FACILITATE BITSTREAMS WITH ALIASES
 - I2C_SODIMMB_SDA
- BOM options provided by this page:
- (NONE)

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DDR3 SO-DIMM CONNECTOR B

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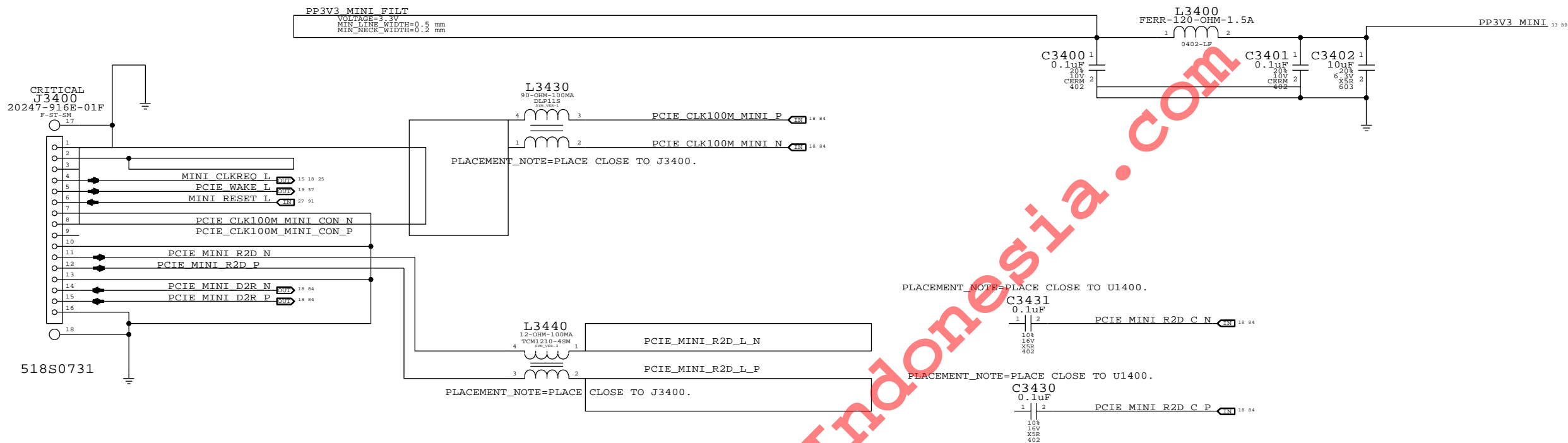
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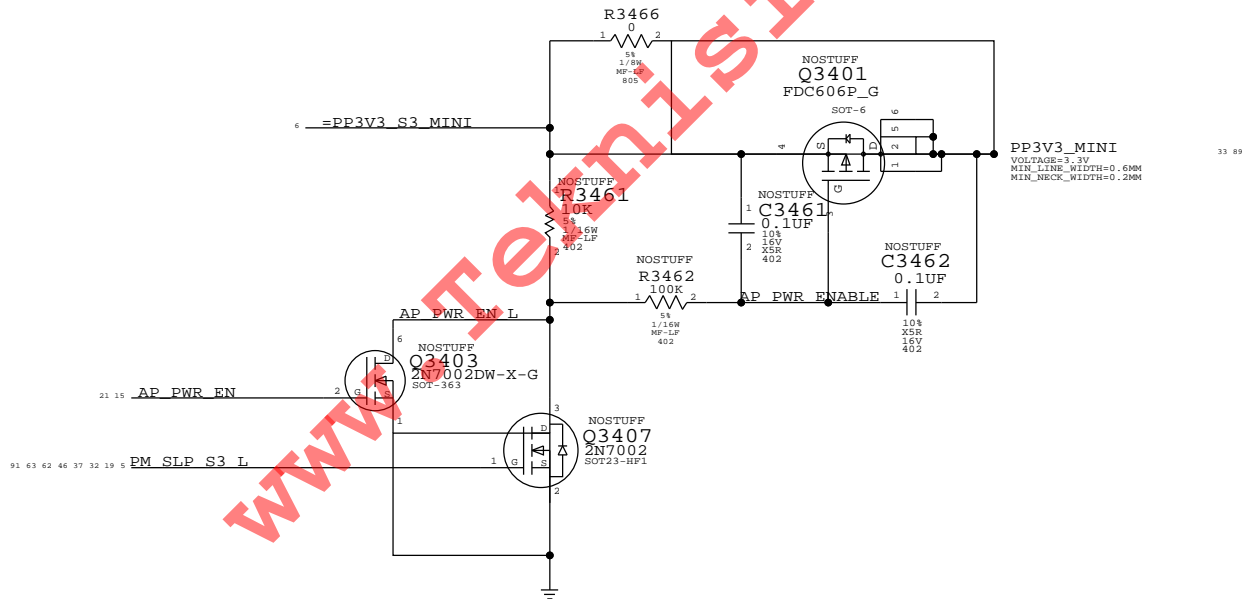
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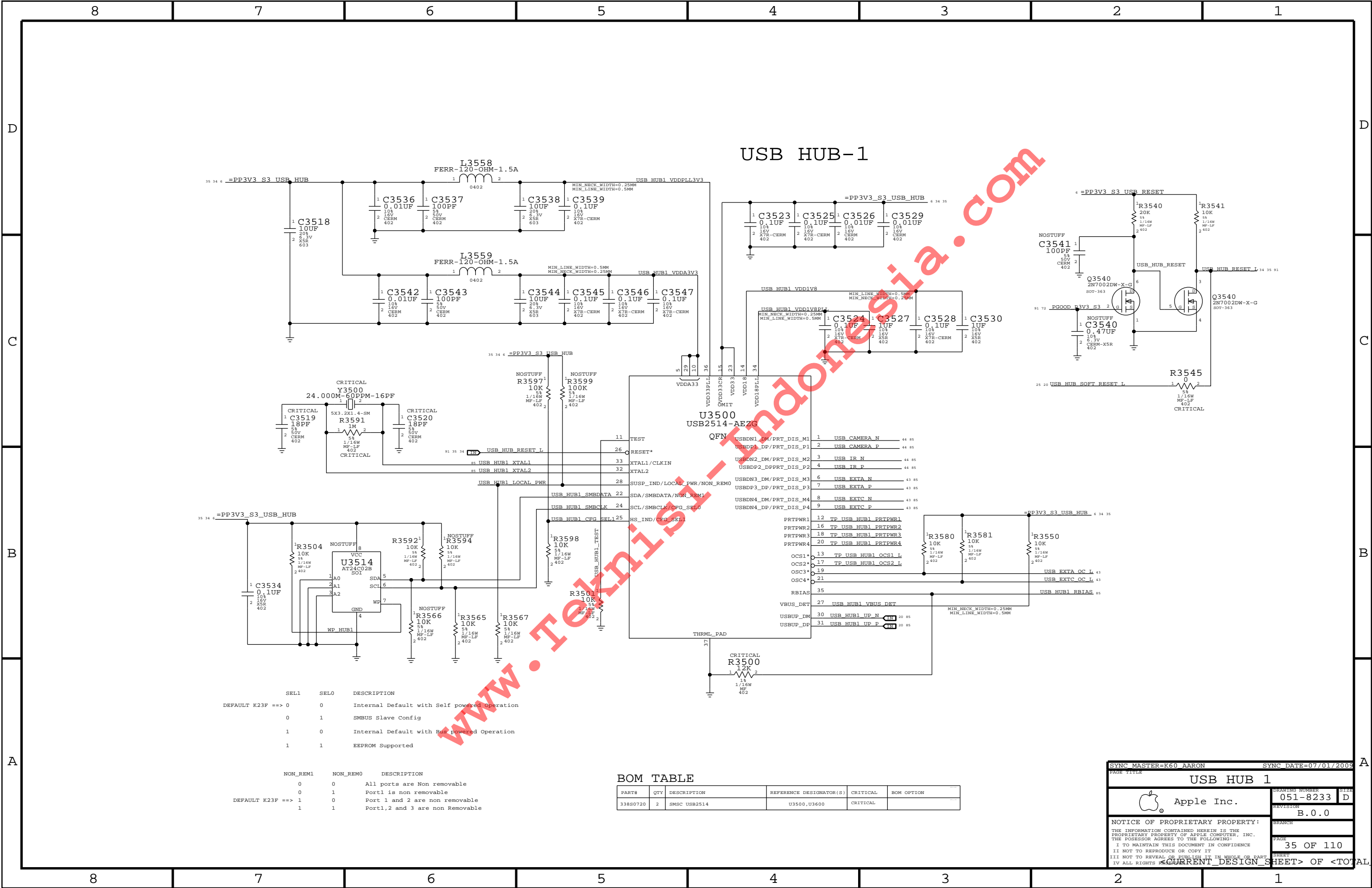


AP POWER ENABLE CIRCUIT

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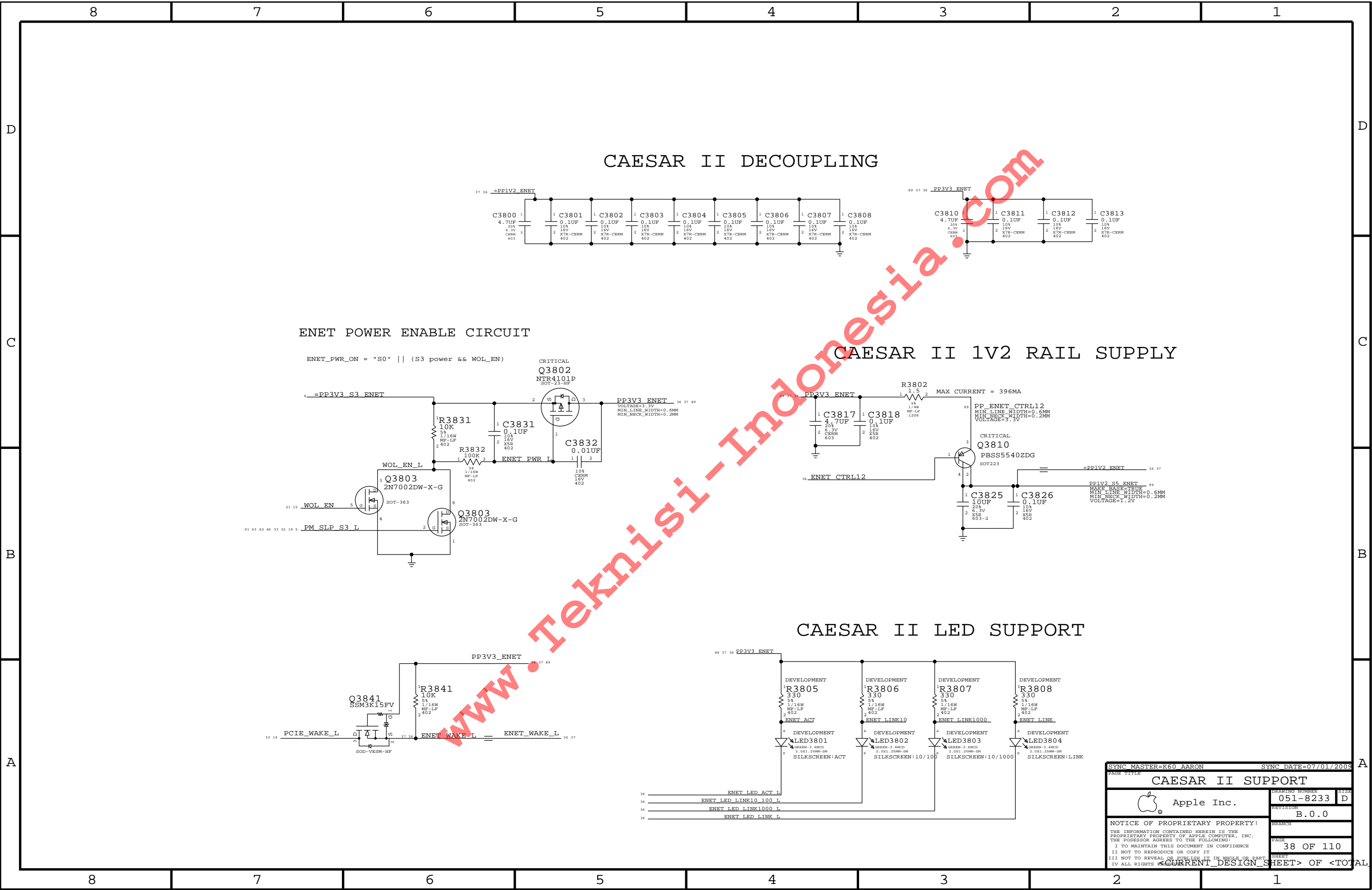



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PCI-E Wireless Connector			
Apple Inc.		051-8233	D
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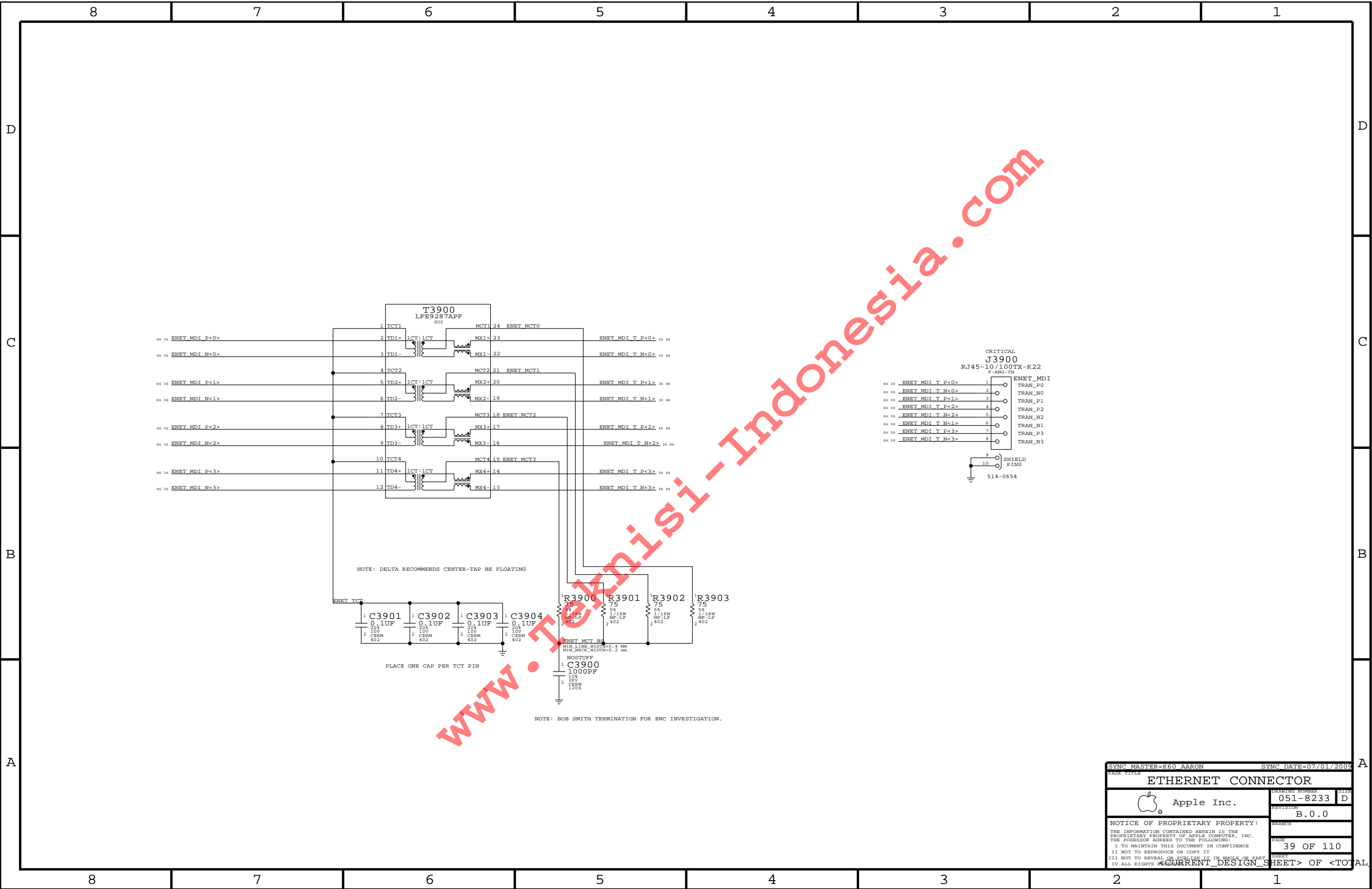



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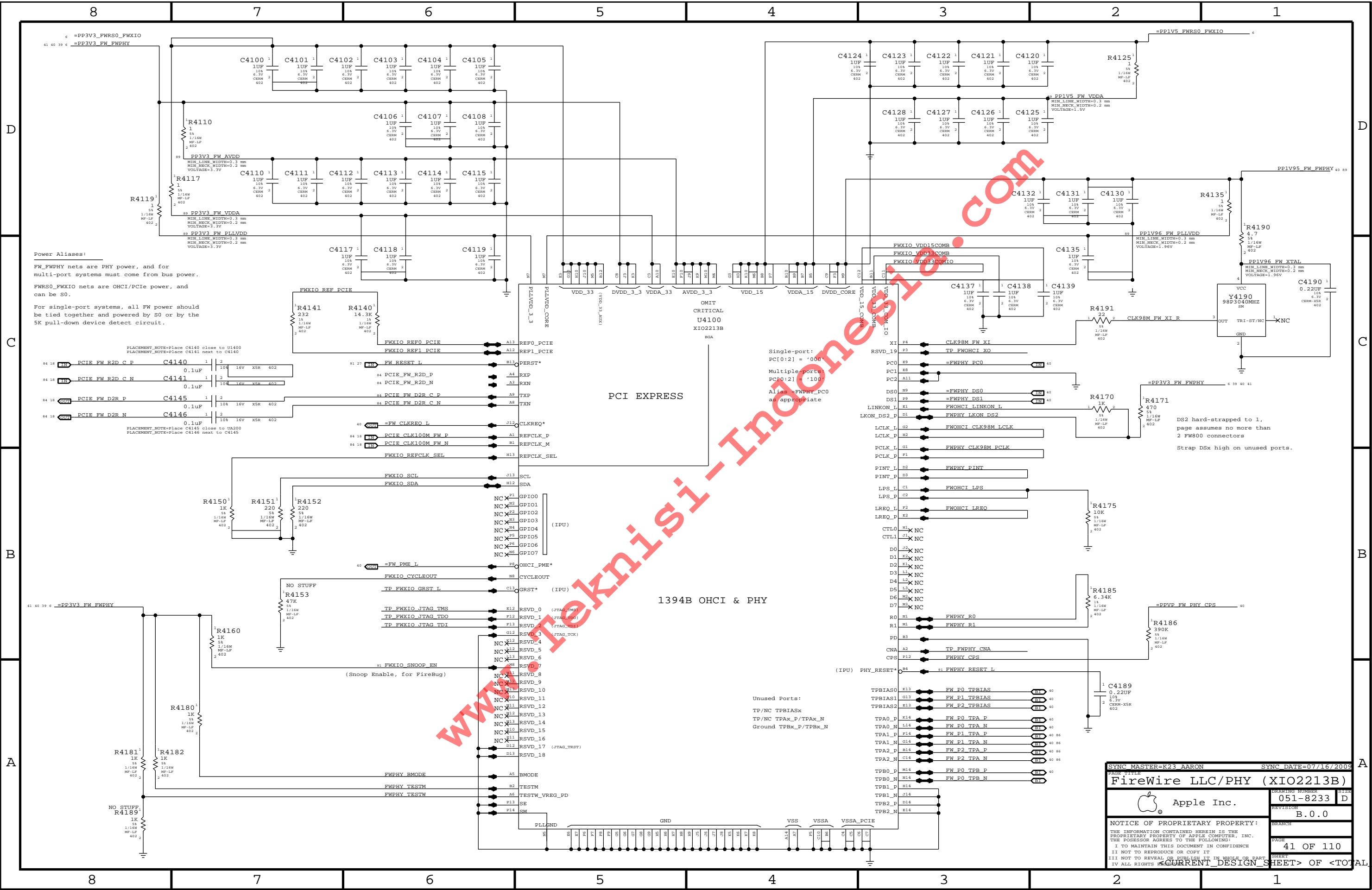
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CAESAR II SUPPORT			
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		BRANCH	
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		SHEET	
		OF <TOTAL>	



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ETHERNET CONNECTOR			
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SYNC DATE=07/16/2009

FireWire LLC/PHY (XIO2213B)

Apple Inc.

051-8233

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41

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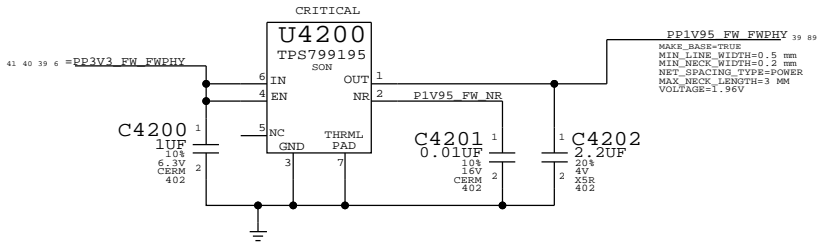
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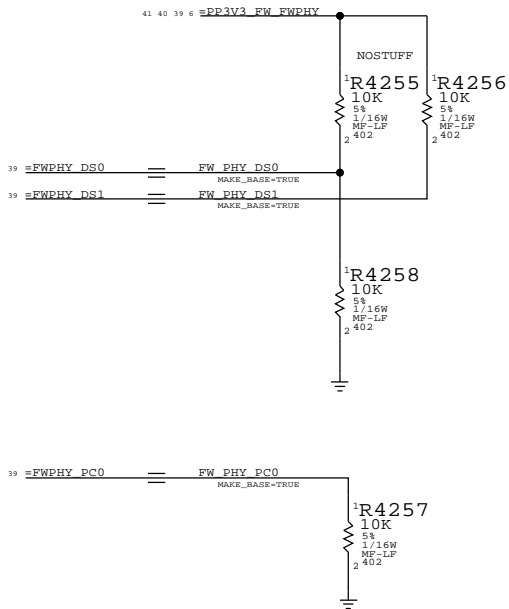
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity



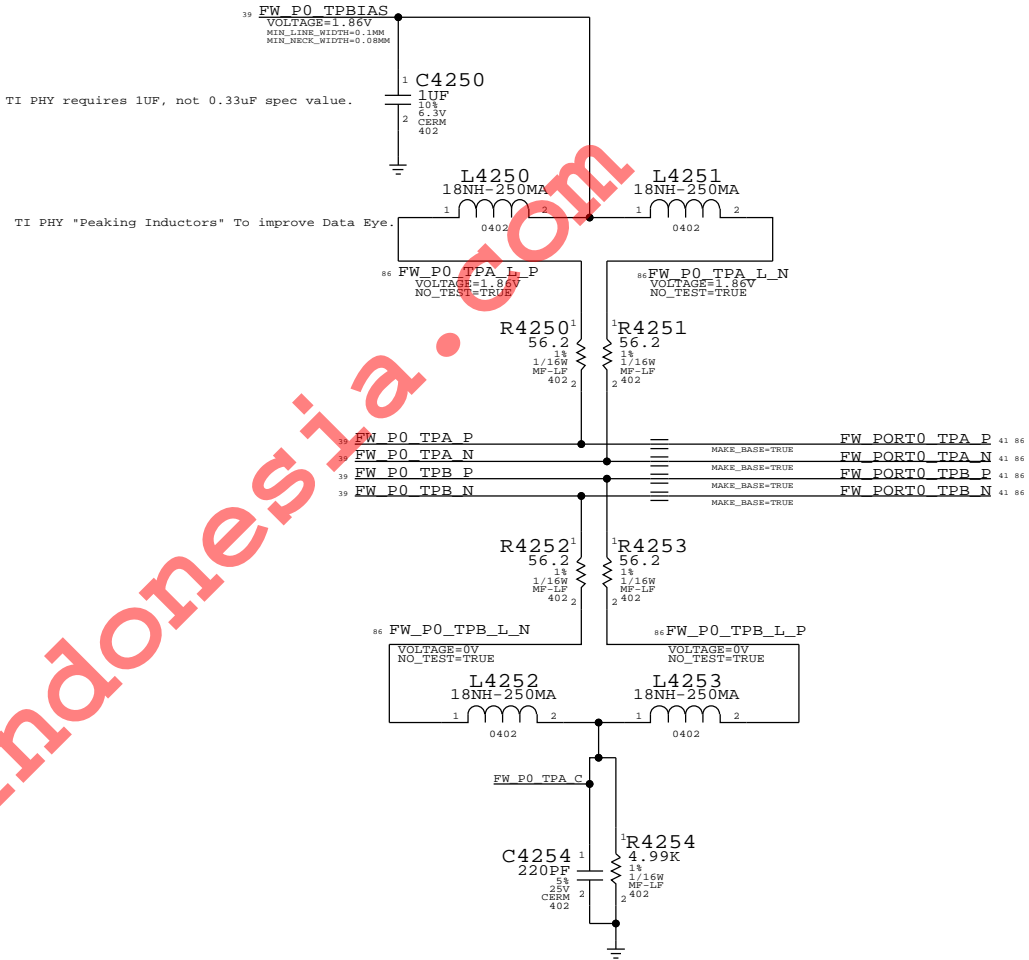
1394 PHY STRAPPING OPTIONS



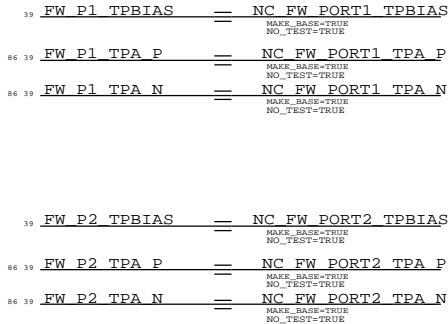
THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

iMacs are now one port only and have Power Code "000"

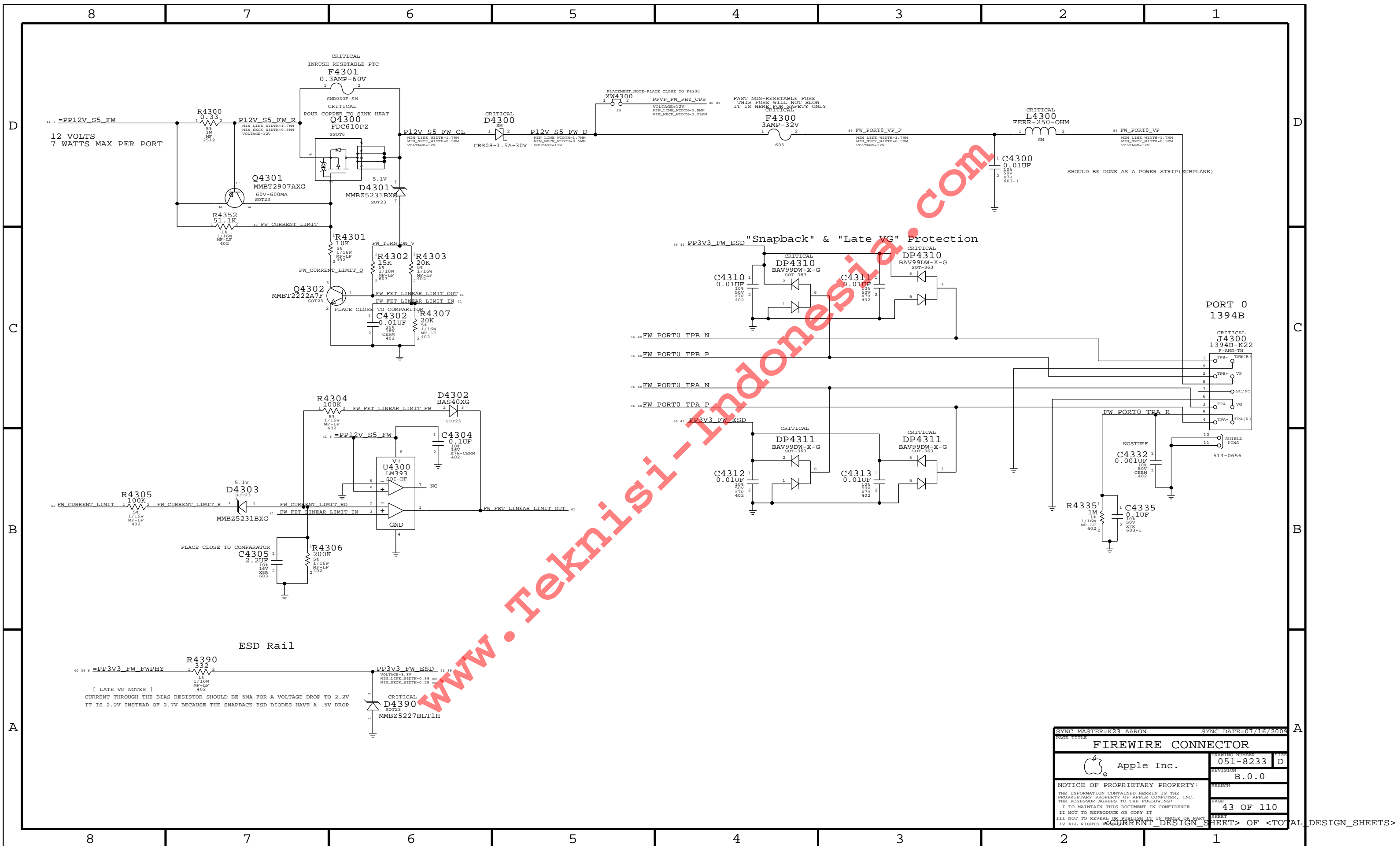
Termination
Place close to FireWire PHY

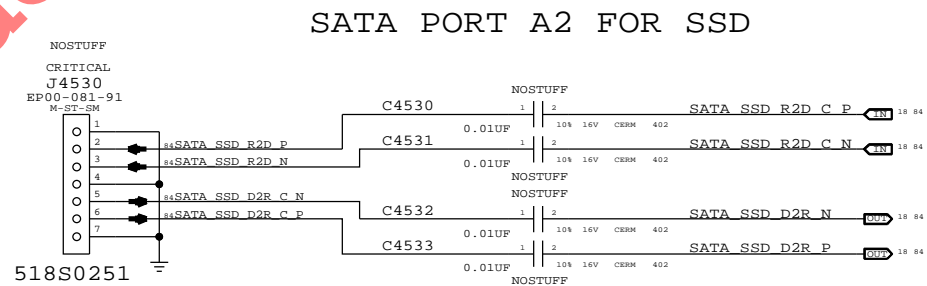
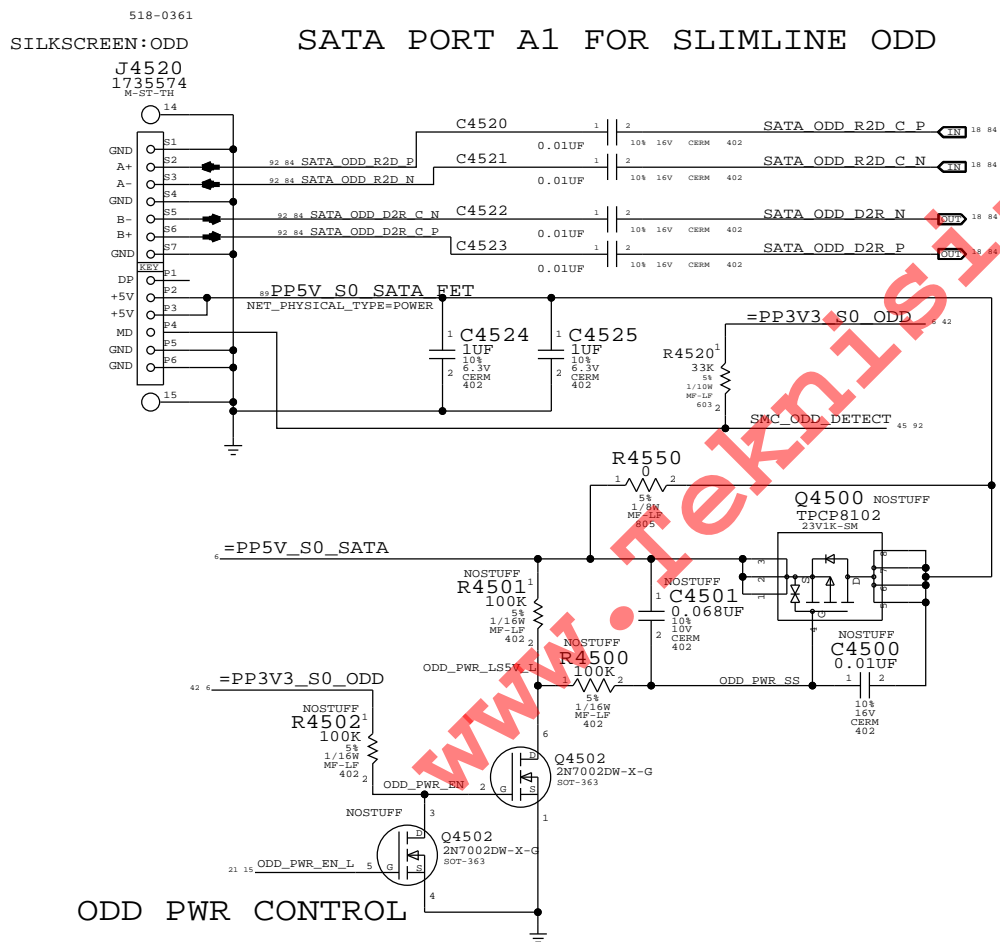
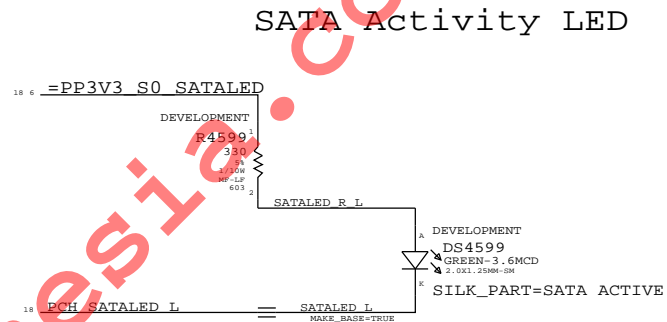
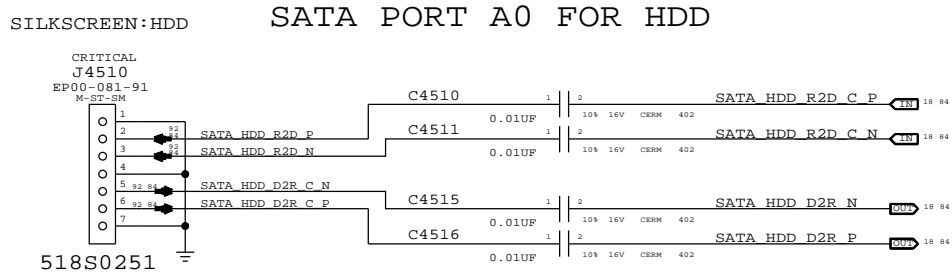


2ND & 3RD TPA/TPB PAIR UNUSED



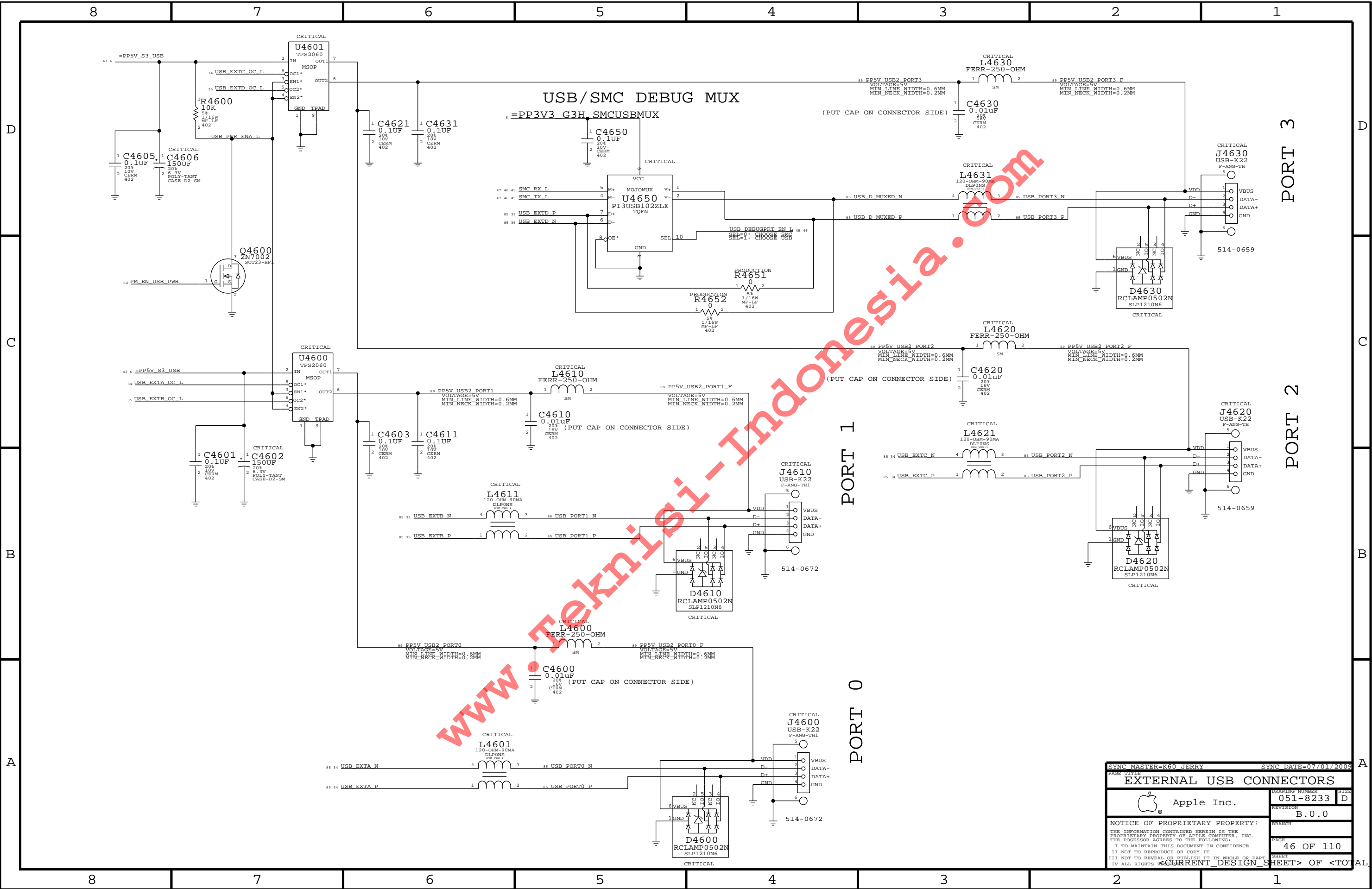
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REVISION		B.0.0			
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PAGE		42 OF 110			
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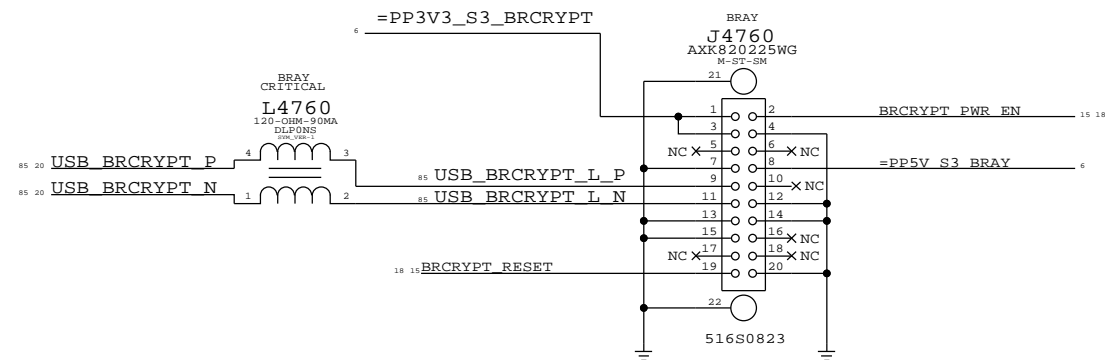
ODD PWR CONTROL

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PAGE TITLE					
SATA Connectors					
Apple Inc.	DRAWING NUMBER	051-8233	D		
	REVISION	B.0.0			
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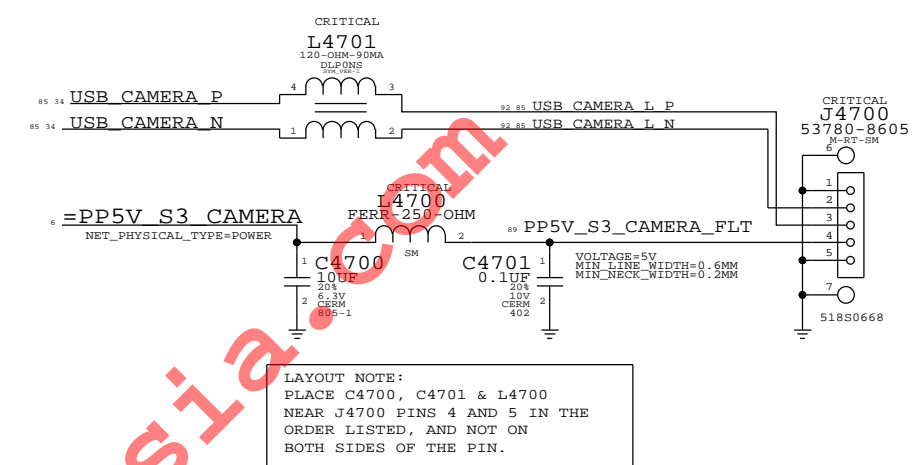


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EXTERNAL USB CONNECTORS			
 Apple Inc.		DRAWING NUMBER 051-8233 D	
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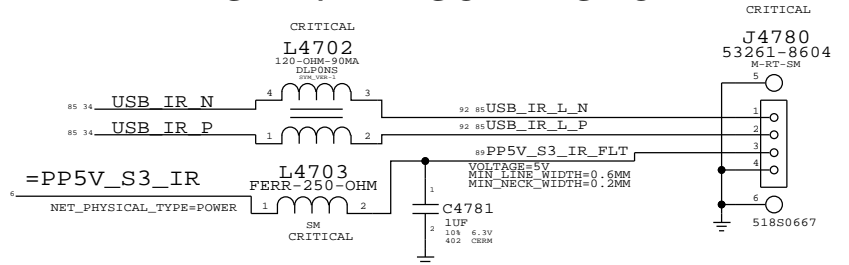
BLURAY DECRYPTOR CONN & FLTR



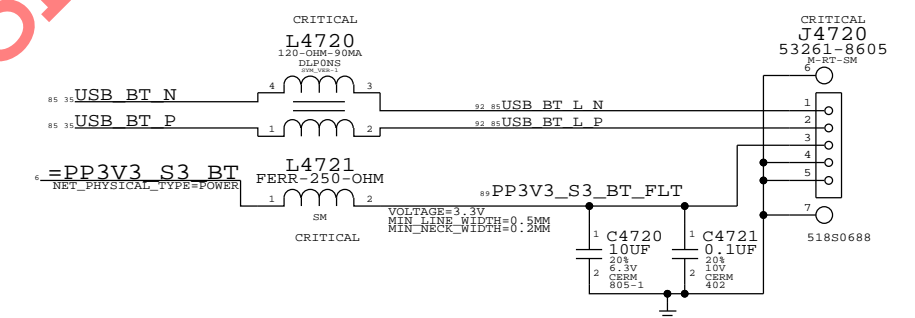
CAMERA CONNECTOR & FILTER



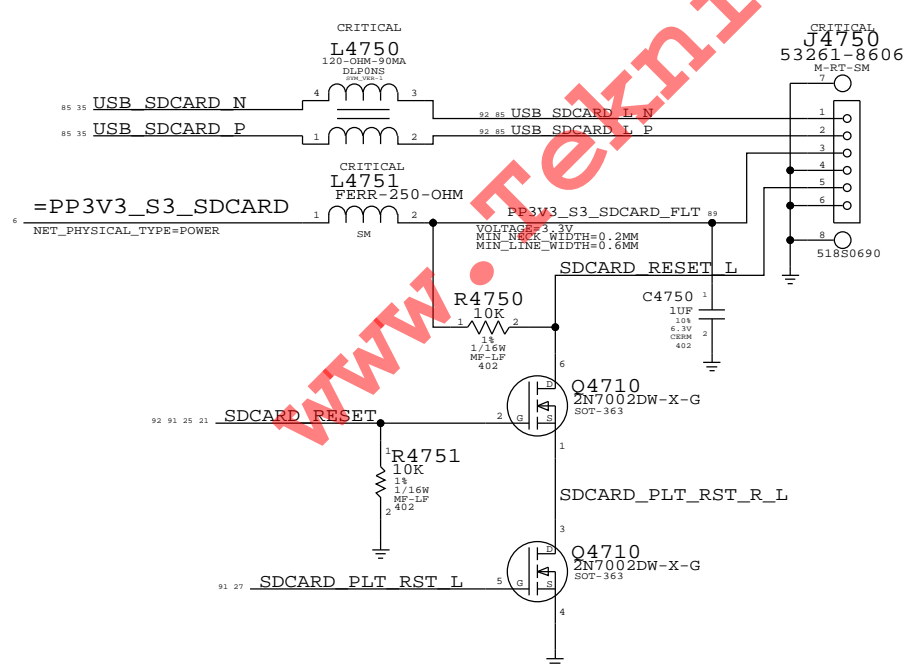
IR RECEIVER CONNECTOR



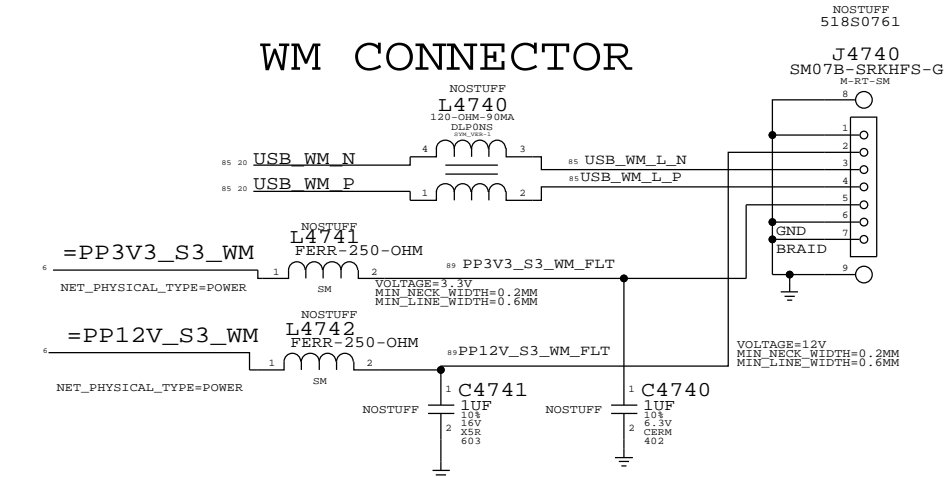
K37L (BLUETOOTH) CONNECTOR




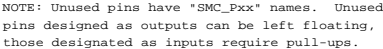
SD Card Reader Board Connector



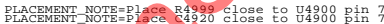
WM CONNECTOR



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Internal USB Connections			
 Apple Inc.		DOCUMENT NUMBER	83424
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		SHEET	
		SHEET# OF <TOTAL>	




```
SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)
```

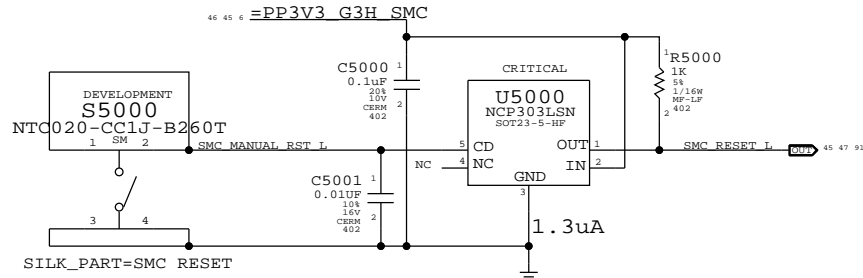


REMOVE R4953/4/5 AFTER PROTO-1

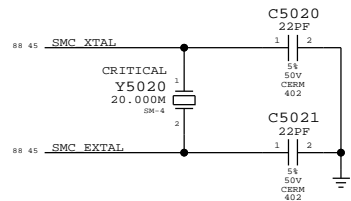
NOTE: SMS Interrupt can be active high or low, rename net accordingly
If SMS interrupt is not used, pull up to SMC rail.

SYNC MASTER=K60 JERRY		SYNC DATE=07/01/2009	
PAGE TITLE			
SMC			
 Apple Inc.	LOCATING NUMBER	051-8233	SIZE D
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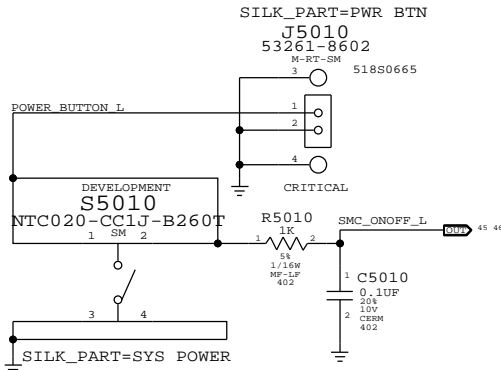
SMC Reset Button / Brownout Detect



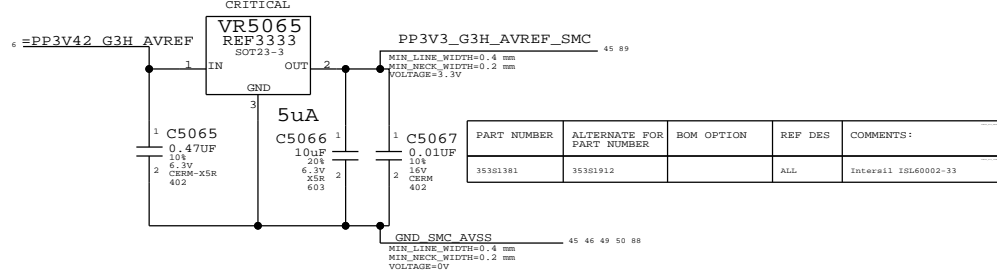
SMC Crystal Circuit



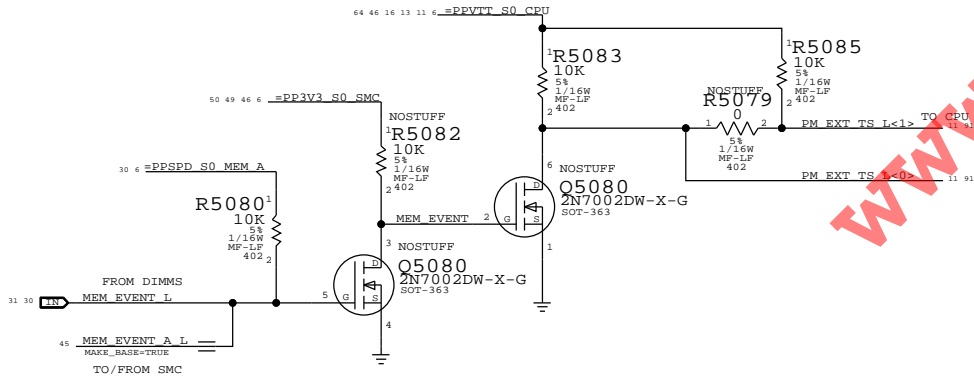
POWER BUTTON



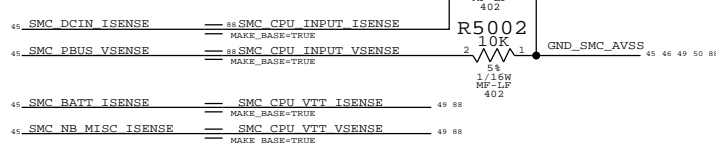
SMC AVREF Supply



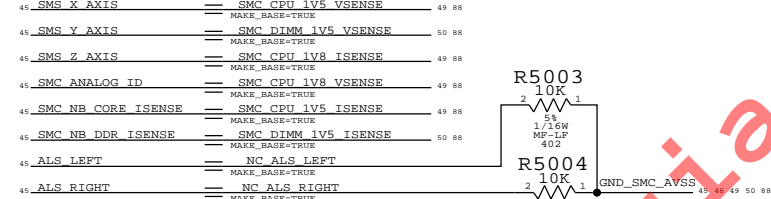
PM_EXTTS_L / MEM_EVENT LEVEL SHIFTING



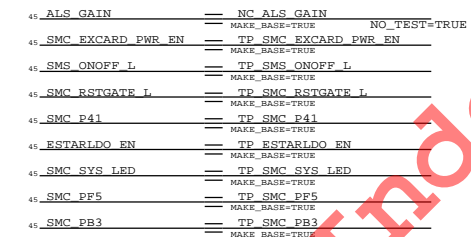
PORT 7 ANALOG SENSORS



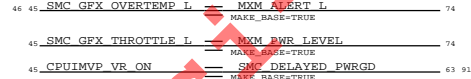
PORT D ANALOG SENSORS (INTERNAL PULLUPS)



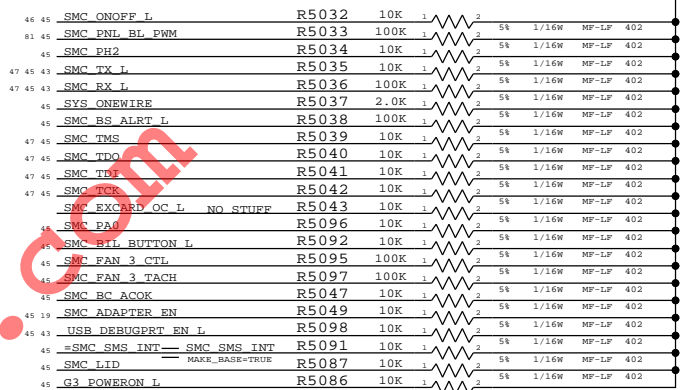
UNUSED TP/NC ALIASES



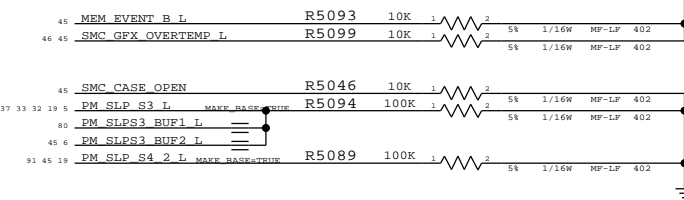
MISC. SIGNAL ALIASES



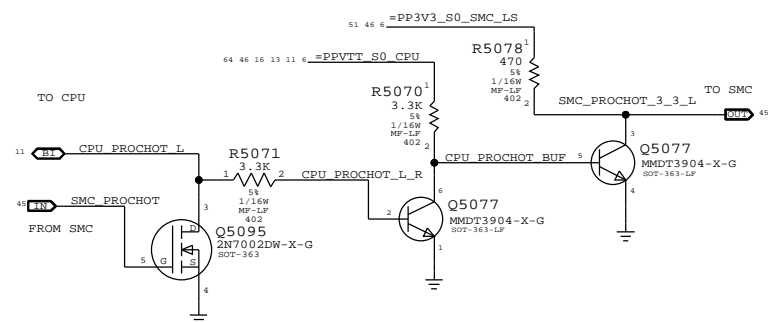
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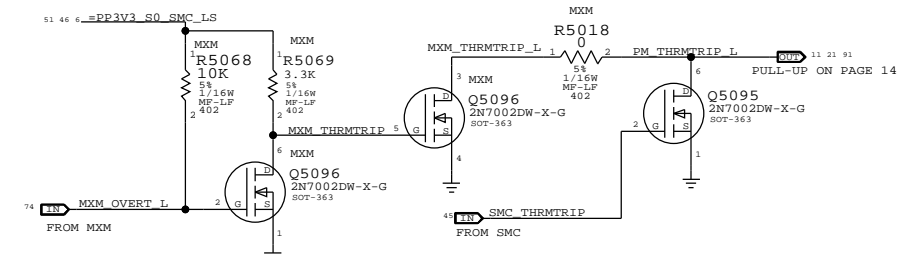
=PP3V3_S0_SMC



SMC PROCHOT 3.3V LEVEL SHIFTING



SMC & MXM THERMTRIP LEVEL SHIFTING



SYNC MASTER=K60 JERRY SYNC DATE=07/01/2009

SMC Support

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CRITICAL CONNECTOR

LPCPLUS
J5100
55909-0374
M-ST-SM

=PP3V3 G3H LPCPLUS
=PP5V S0 LPCPLUS

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34

LPC CLK33M LPCPLUS
LPC AD<0>
LPC AD<1>
LPC AD<2>
LPC AD<3>
SPI ALT MOSI
SPI ALT MISO
LPC FRAME L
PM CLKRUN L
SMC TMS
DEBUG RESET L
SMC TDO
SMC TRST L
SMC MD1
SMC TX L
SPIROM_USE MLB
SPI ALT CLK
SPI ALT CS L
LPC SERIO
LPC PWRDWN L
SMC TDI
SMC TCK
SMC RESET L
SMC NMI
SMC RX L
LPCPLUS GPIO

21 27 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

516S0573

The schematic diagram illustrates the internal circuitry of the LPC1114 evaluation board. Key components include:

- U5100 (LPC1114):** The main microcontroller, shown in a pinout view with pins 1 through 10 labeled. It is connected to various external components.
- U5146 (PRODUCTION):** A production version of the microcontroller, shown in a pinout view with pins 1 through 10 labeled. It is connected to various external components.
- Resistors:** R5144 (20K), R5145 (10K), R5146 (10K), R5147 (10K), R5148 (10K), R5149 (10K), R5150 (10K), R5151 (10K), R5152 (10K), R5153 (10K), R5154 (10K), R5155 (10K), R5156 (10K), R5157 (10K), R5158 (10K), R5159 (10K), R5160 (10K), R5161 (10K), R5162 (10K), R5163 (10K), R5164 (10K), R5165 (10K), R5166 (10K), R5167 (10K), R5168 (10K), R5169 (10K), R5170 (10K), R5171 (10K), R5172 (10K), R5173 (10K), R5174 (10K), R5175 (10K), R5176 (10K), R5177 (10K), R5178 (10K), R5179 (10K), R5180 (10K), R5181 (10K), R5182 (10K), R5183 (10K), R5184 (10K), R5185 (10K), R5186 (10K), R5187 (10K), R5188 (10K), R5189 (10K), R5190 (10K), R5191 (10K), R5192 (10K), R5193 (10K), R5194 (10K), R5195 (10K), R5196 (10K), R5197 (10K), R5198 (10K), R5199 (10K), R5200 (10K), R5201 (10K), R5202 (10K), R5203 (10K), R5204 (10K), R5205 (10K), R5206 (10K), R5207 (10K), R5208 (10K), R5209 (10K), R5210 (10K), R5211 (10K), R5212 (10K), R5213 (10K), R5214 (10K), R5215 (10K), R5216 (10K), R5217 (10K), R5218 (10K), R5219 (10K), R5220 (10K), R5221 (10K), R5222 (10K), R5223 (10K), R5224 (10K), R5225 (10K), R5226 (10K), R5227 (10K), R5228 (10K), R5229 (10K), R5230 (10K), R5231 (10K), R5232 (10K), R5233 (10K), R5234 (10K), R5235 (10K), R5236 (10K), R5237 (10K), R5238 (10K), R5239 (10K), R5240 (10K), R5241 (10K), R5242 (10K), R5243 (10K), R5244 (10K), R5245 (10K), R5246 (10K), R5247 (10K), R5248 (10K), R5249 (10K), R5250 (10K), R5251 (10K), R5252 (10K), R5253 (10K), R5254 (10K), R5255 (10K), R5256 (10K), R5257 (10K), R5258 (10K), R5259 (10K), R5260 (10K), R5261 (10K), R5262 (10K), R5263 (10K), R5264 (10K), R5265 (10K), R5266 (10K), R5267 (10K), R5268 (10K), R5269 (10K), R5270 (10K), R5271 (10K), R5272 (10K), R5273 (10K), R5274 (10K), R5275 (10K), R5276 (10K), R5277 (10K), R5278 (10K), R5279 (10K), R5280 (10K), R5281 (10K), R5282 (10K), R5283 (10K), R5284 (10K), R5285 (10K), R5286 (10K), R5287 (10K), R5288 (10K), R5289 (10K), R5290 (10K), R5291 (10K), R5292 (10K), R5293 (10K), R5294 (10K), R5295 (10K), R5296 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Timing diagram for SPI signals (CLK, MOSI, MISO) showing setup and hold times relative to R5156 and R5157.

Signals shown: SPI ALT CLK, SPI ALT MOSI, SPI ALT MISO.


Timing annotations:

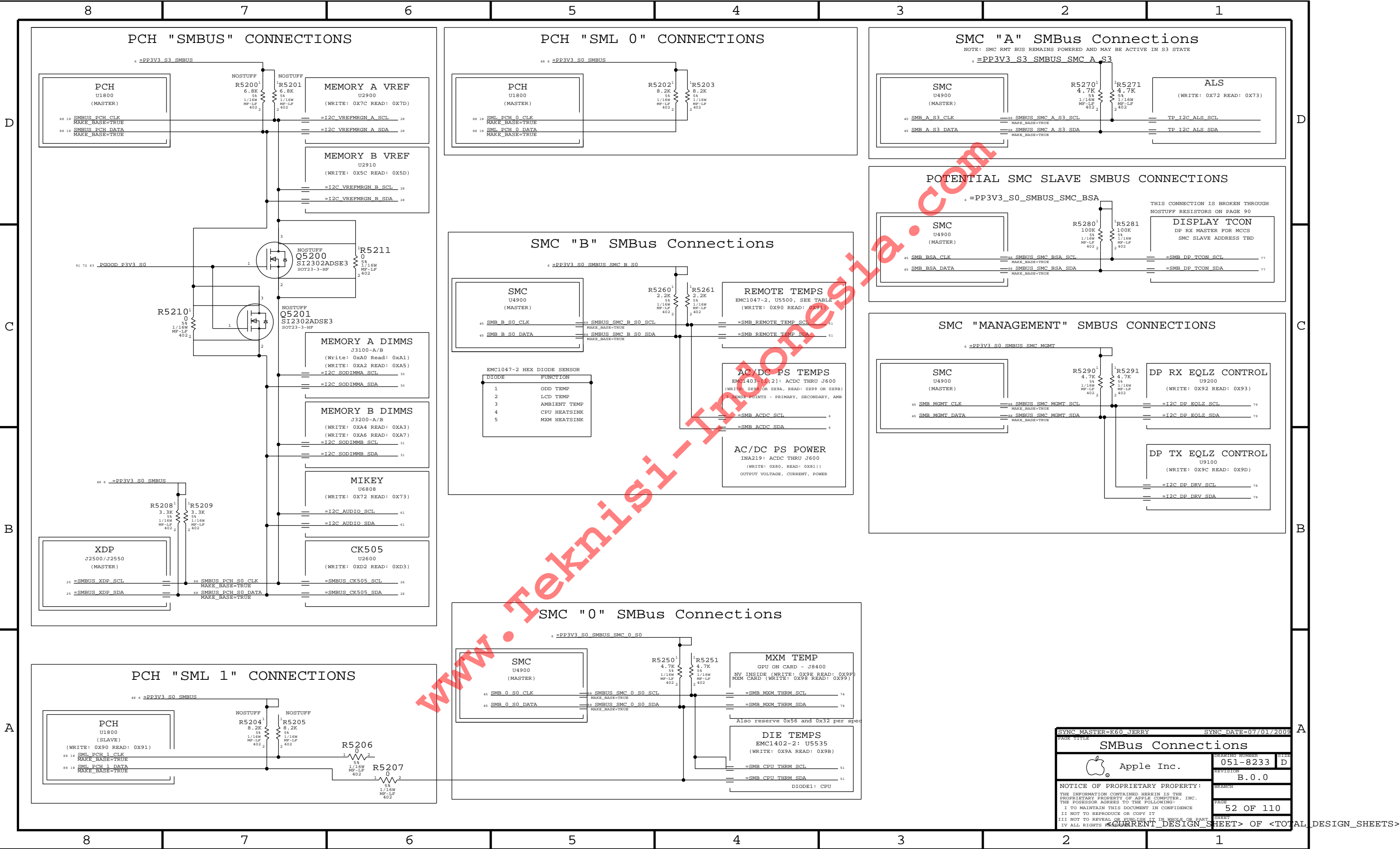
- 1: Setup time (ns)
- 2: Hold time (ns)
- 5k: Delay (ns)
- 1/16W: Delay (ns)
- NF+LP: Delay (ns)
- 402: Delay (ns)

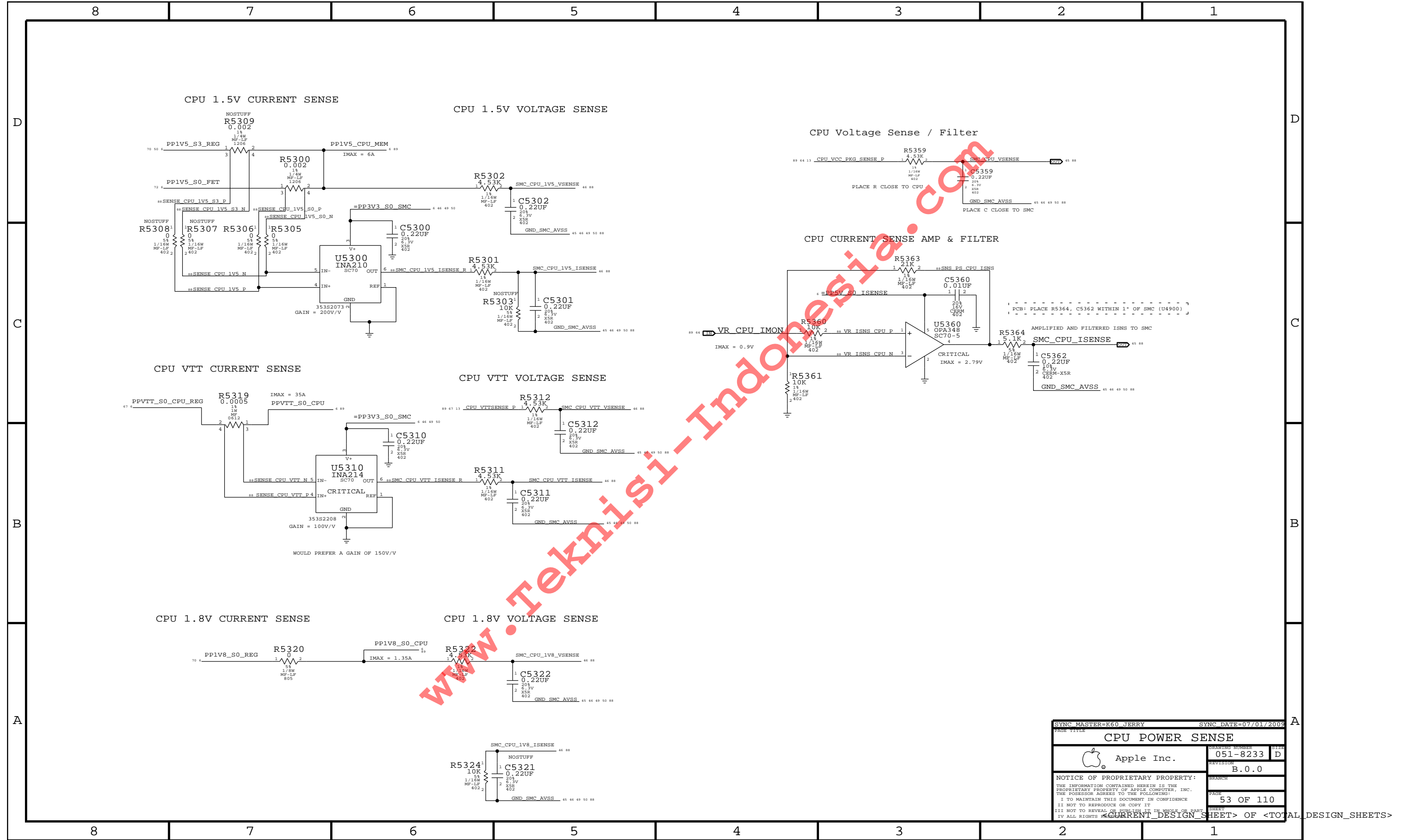
Placement notes:

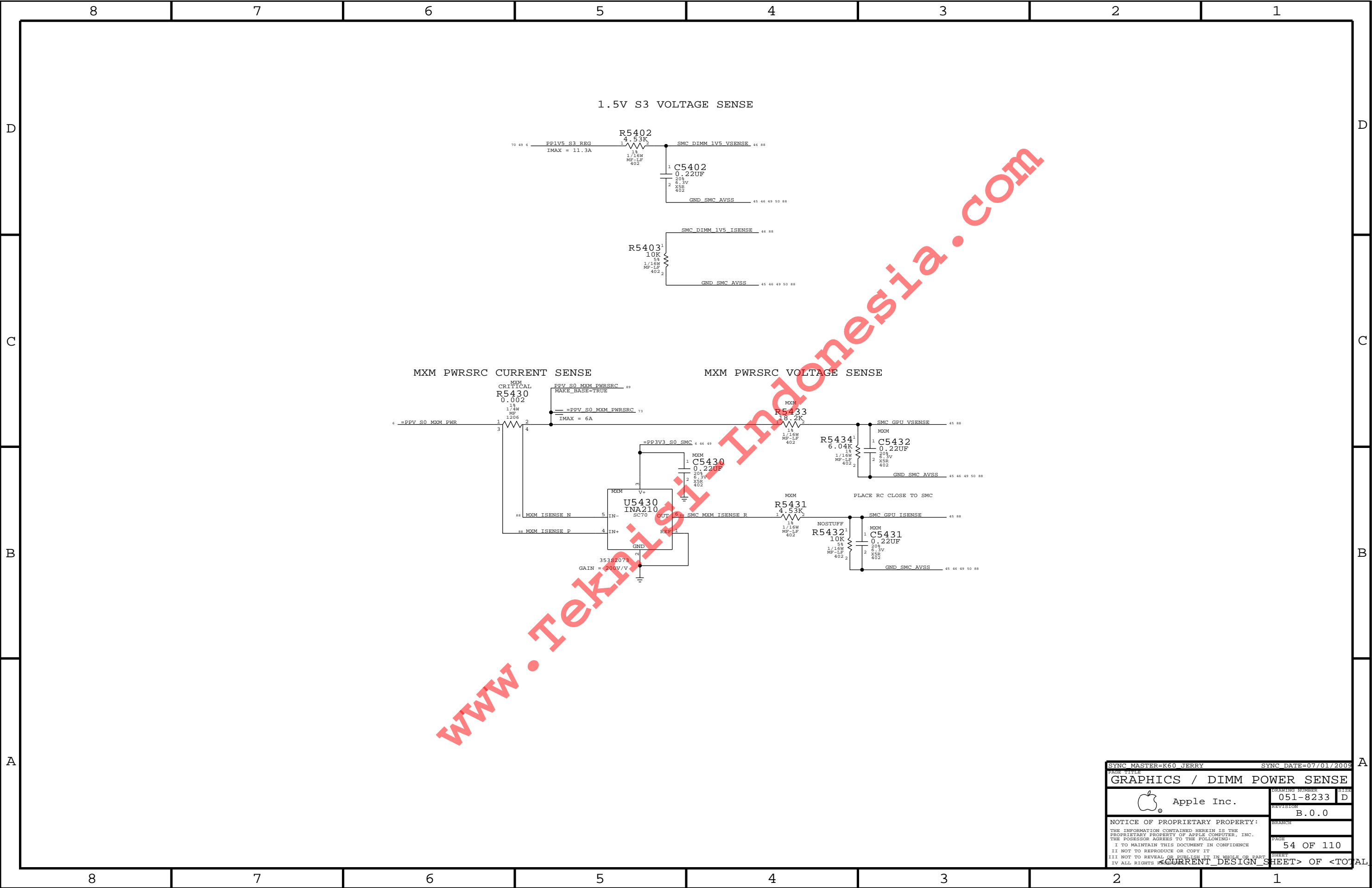
- PLACEMENT_NOTE=Place next to R6150
- PLACEMENT_NOTE=Place next to R6152
- PLACEMENT_NOTE=Place next to R6105

Watermark: WWW

SYNCH MASTER=K60 SIJI		SYNCH DATE=07/01/2005	
PAGE 111			
LPC+SPI Debug Connector			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8233		D
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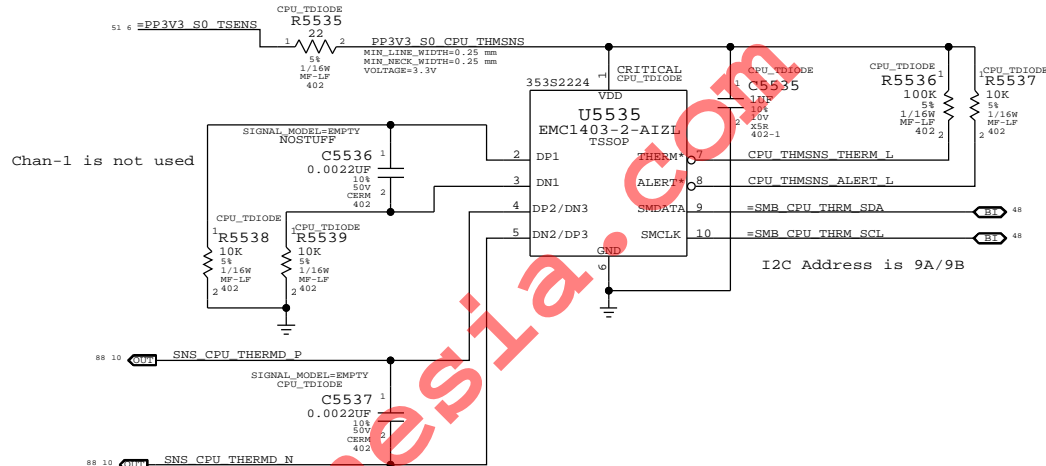
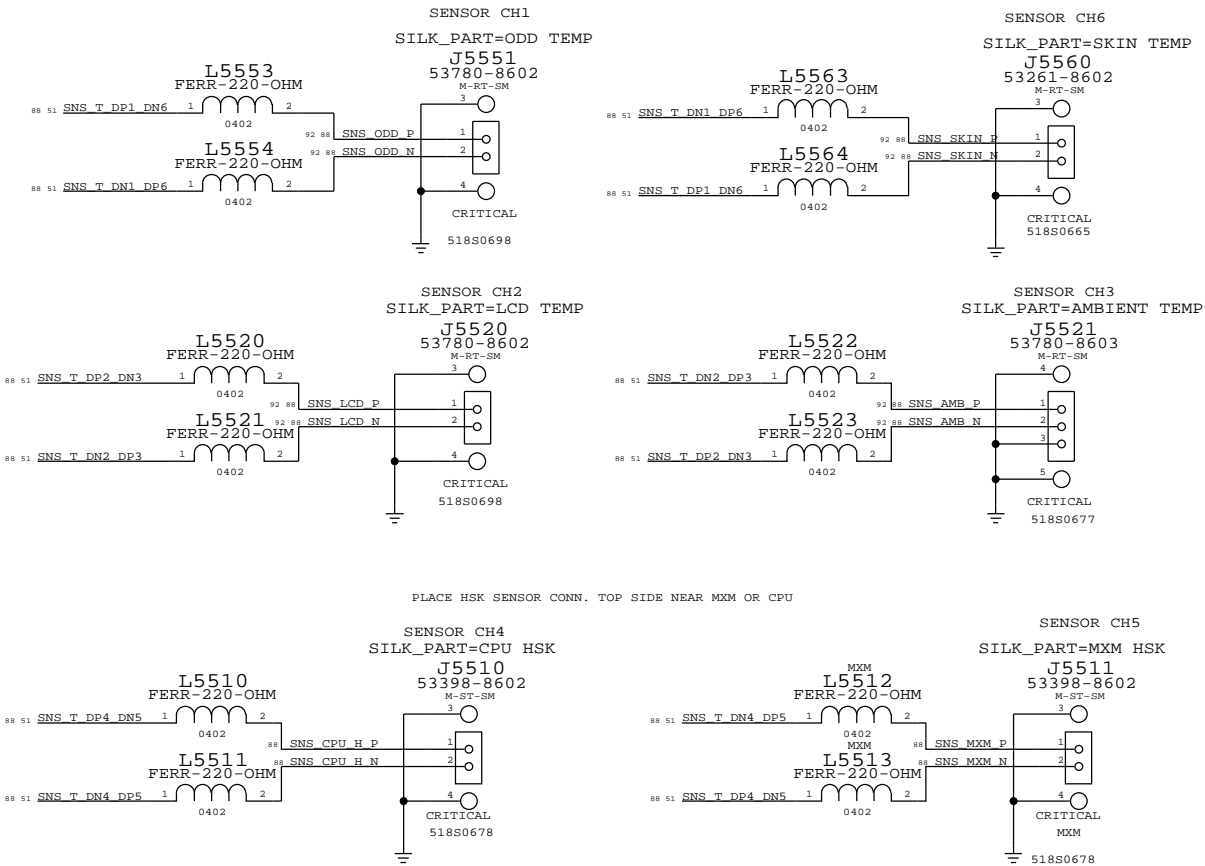






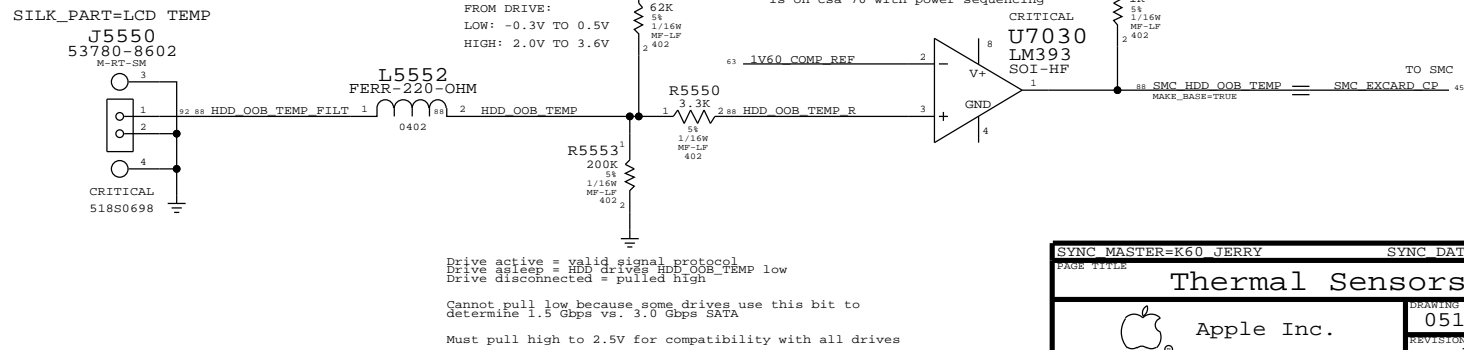
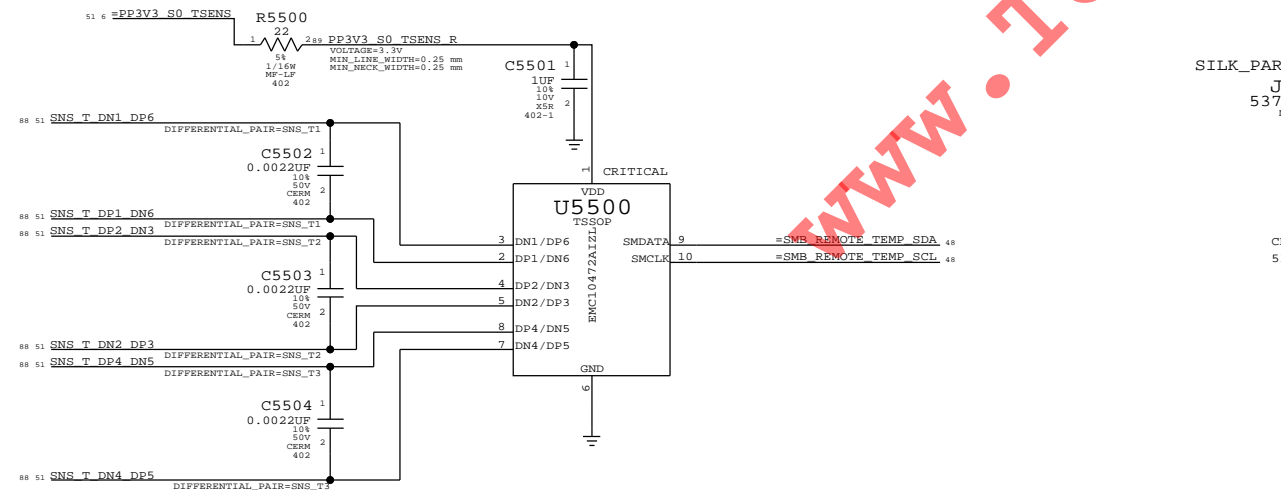
REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD

CPU T-DIODE THERMAL SENSOR

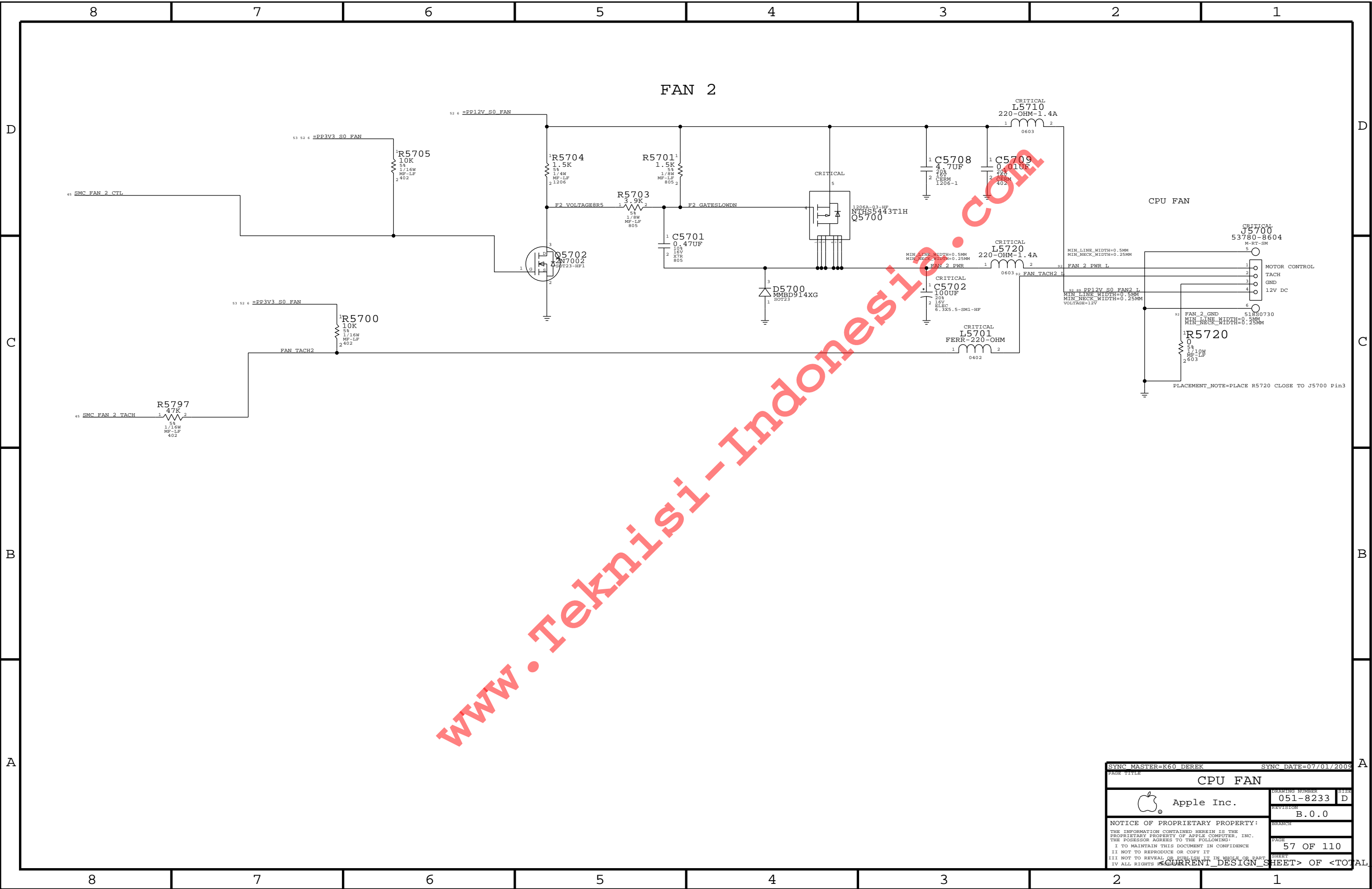



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)

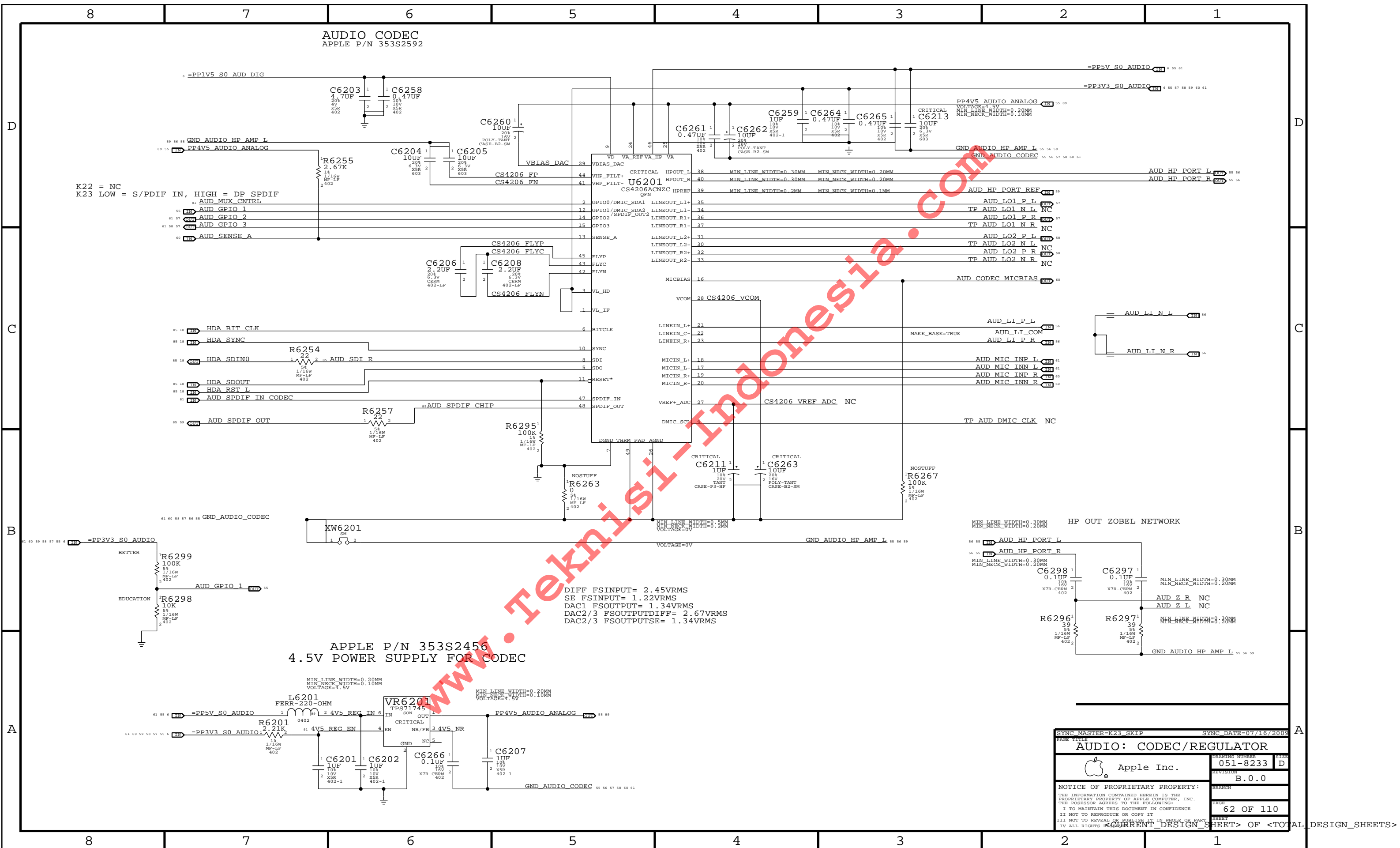
HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



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PAGE TITLE		Thermal Sensors	
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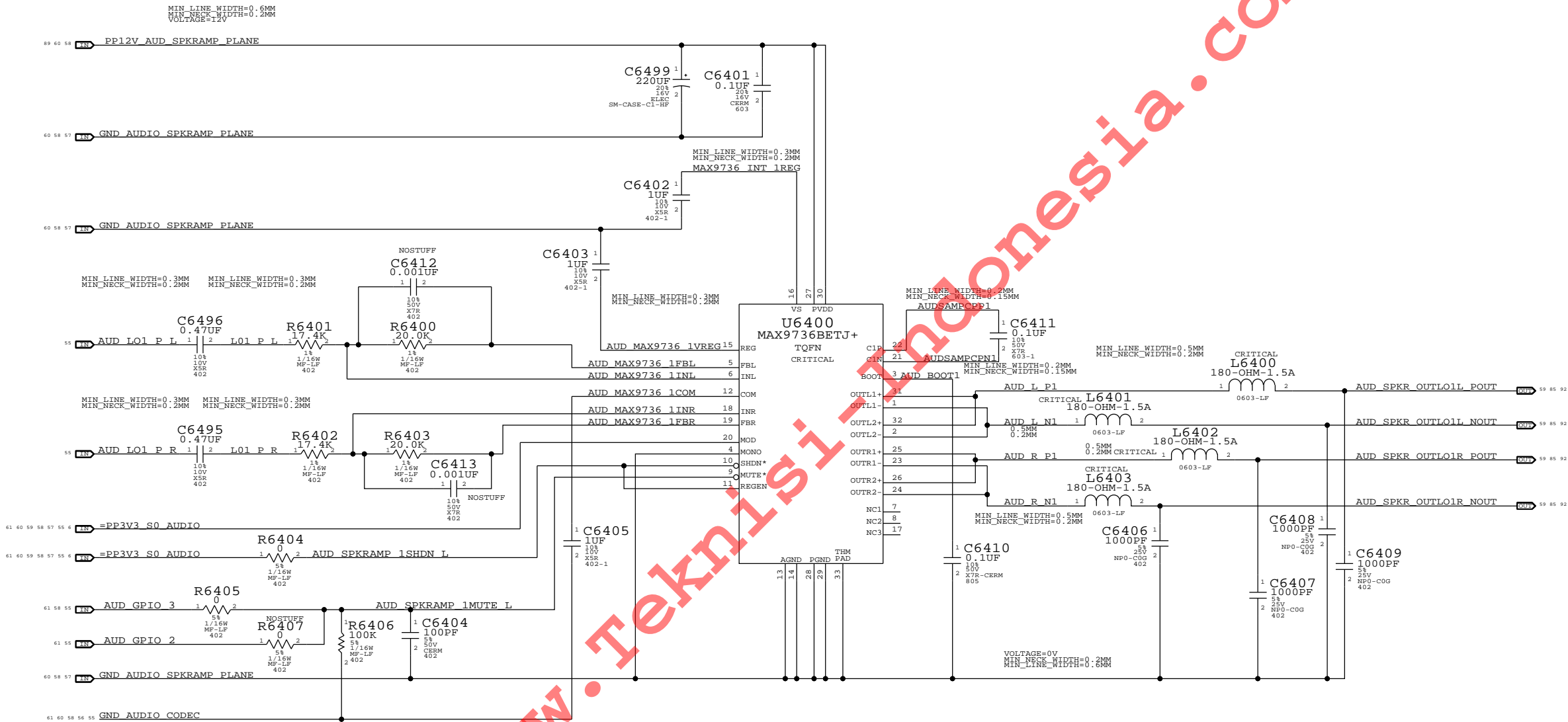



SYNC MASTER=K60 DEREK		SYNC DATE=07/01/2009	
PAGE TITLE			
CPU FAN			
	DRAWING NUMBER		81242
	051-8233		D
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TWEETER SPEAKER AMPLIFIER
MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K) TURN ON TIME: 110MS
CODEC OUT = 1.335VRMS TURN ON DELAY: 150MS
AMP VOUT = 7.355VRMS RIN = 17.4 OHMS
FC = 19.5 HZ
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

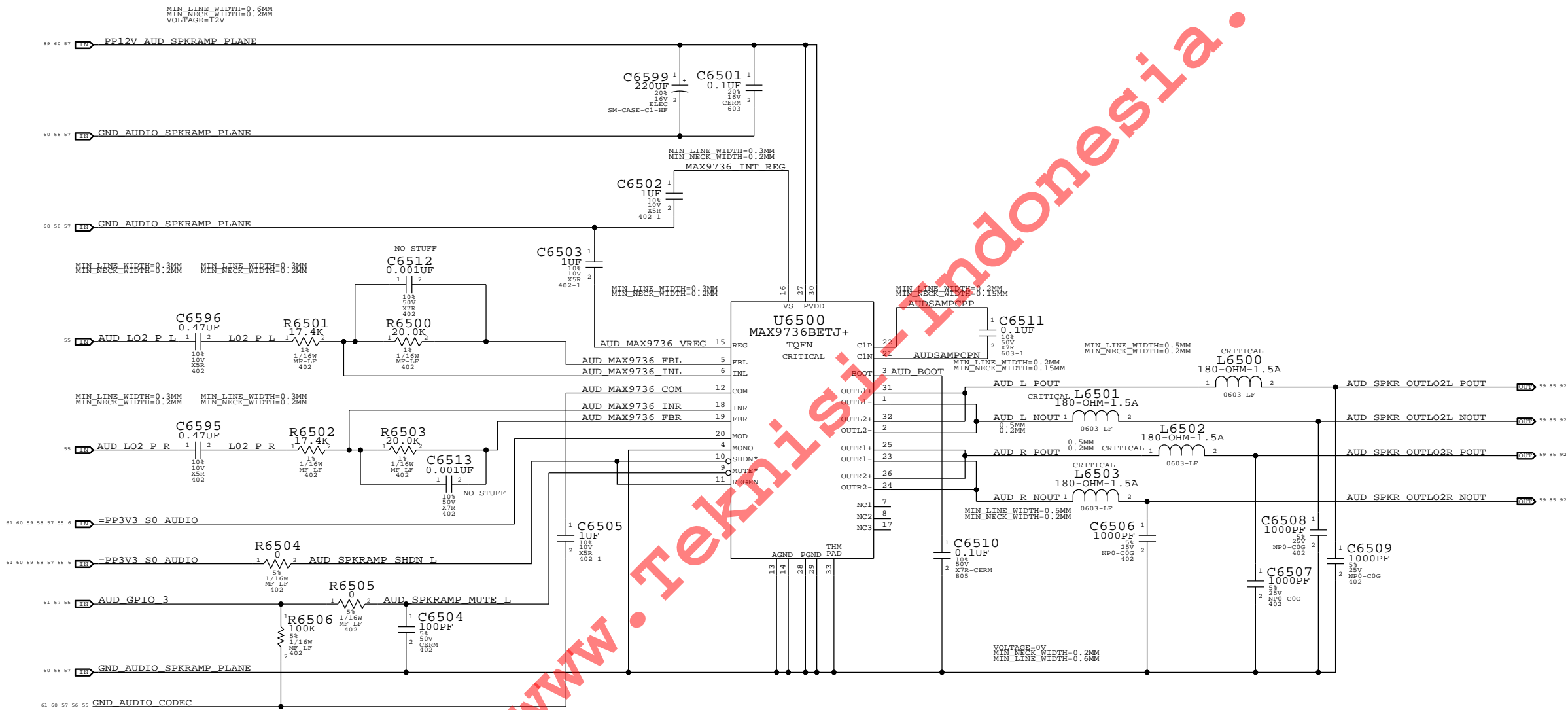


SYNC MASTER=K23 SKIP		SYNC DATE=07/16/2009	
PAGE TITLE			
AUDIO: Tweeter Amp 1			
 Apple Inc.		MANAGING NUMBER 051-8233	SHEET D
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WOOFER SPEAKER AMPLIFIER

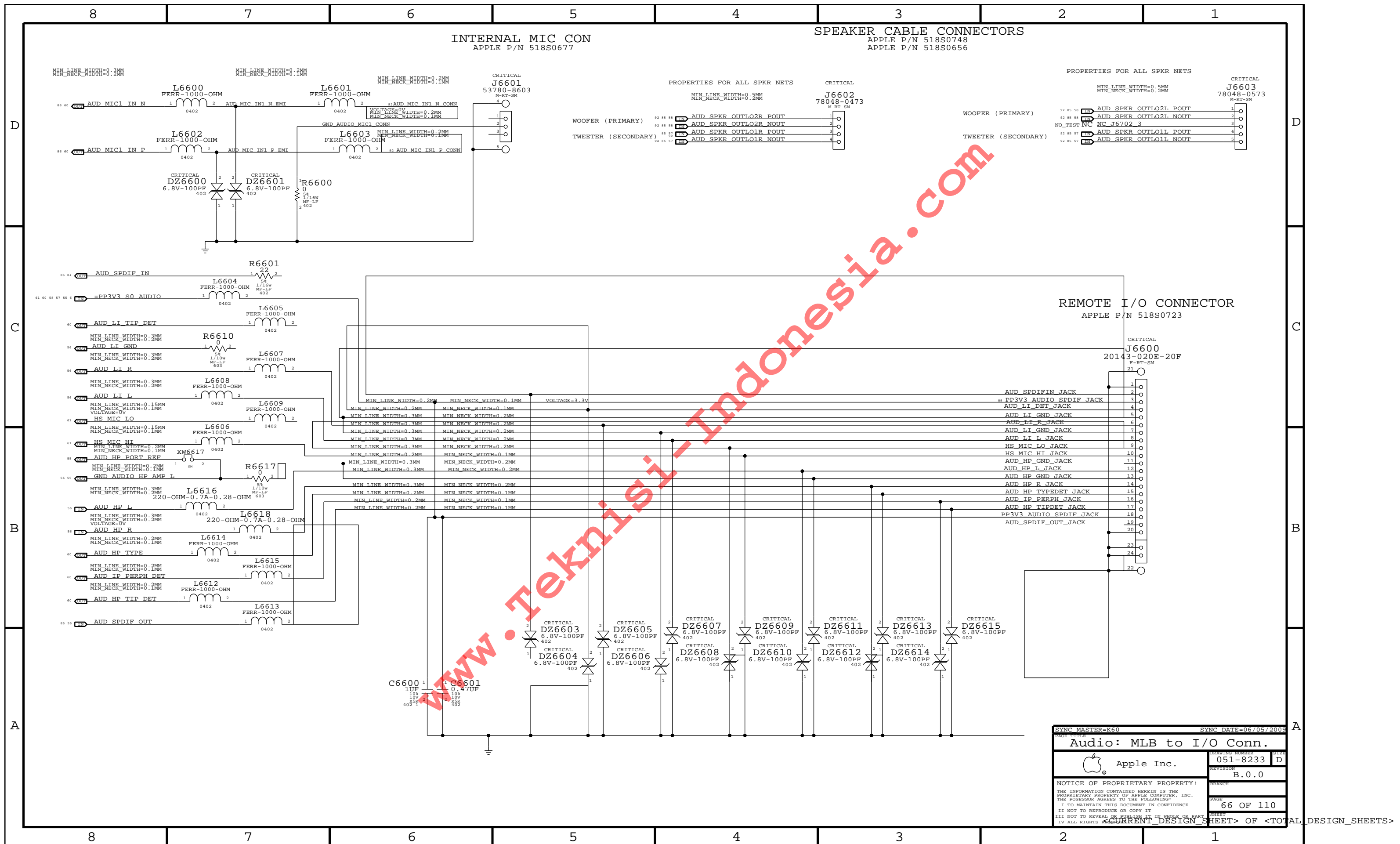
MAX9736B APN:353S2042

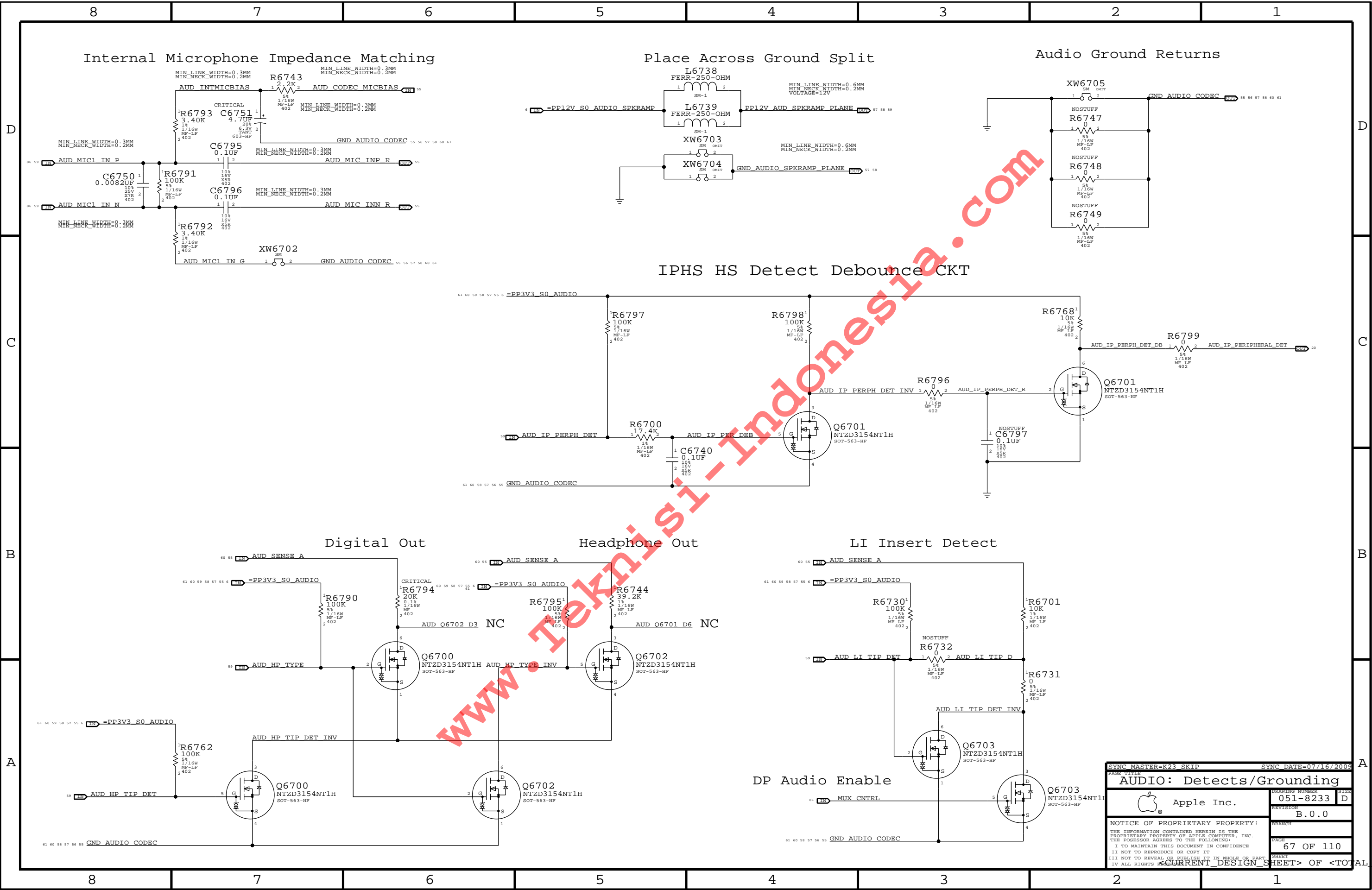
GAIN = -4.8(20K/17.4K) TURN ON TIME: 110MS
CODEC OUT = 1.335VRMS TURN ON DELAY: 150MS
AMP VOUT = 7.355VRMS RIN = 17.4 OHMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N FC = 19.5 HZ




PAGE TITLE		PAGE NUMBER	
AUDIO: Woofer Amp		051-8233 D	
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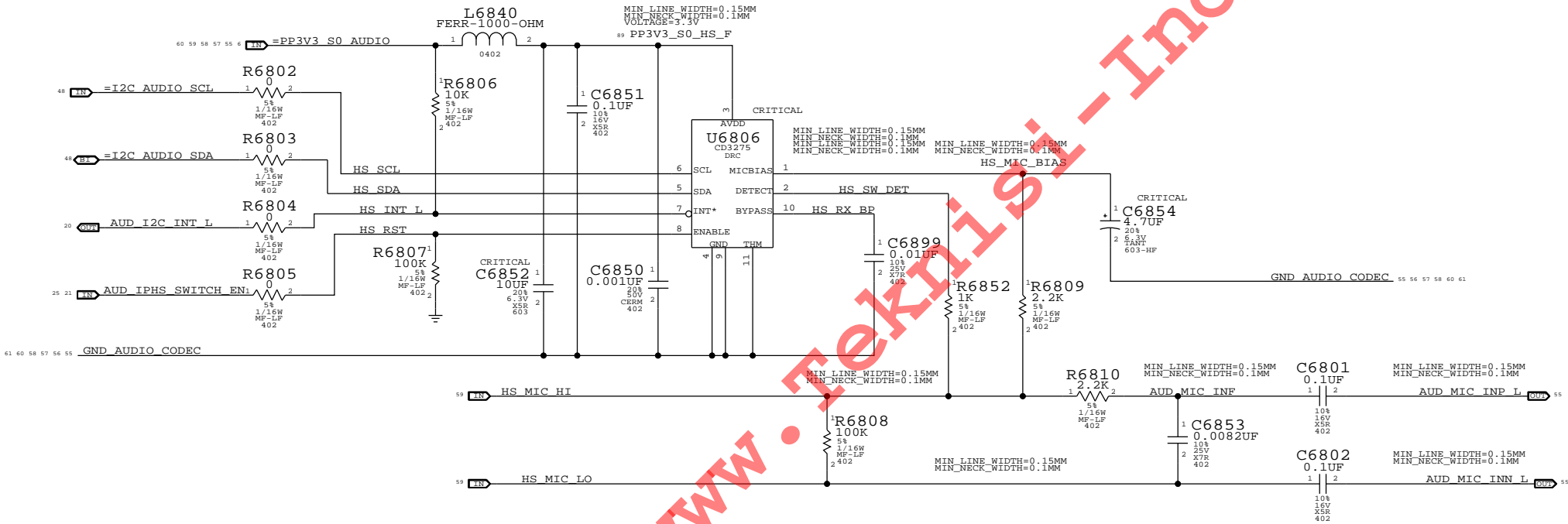


SYNC MASTER=K23 SKIP		SYNC DATE=07/16/2009	
PAGE TITLE			
AUDIO: Detects/Grounding			
 Apple Inc.	DESIGN NUMBER	051-8233	D
	REVISION	B.0.0	
	BRANCH		
PAGE			
67 OF 110			
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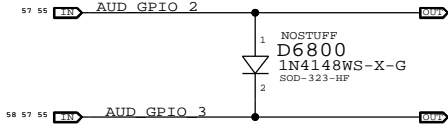
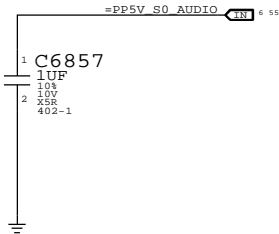
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/ INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D (13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256

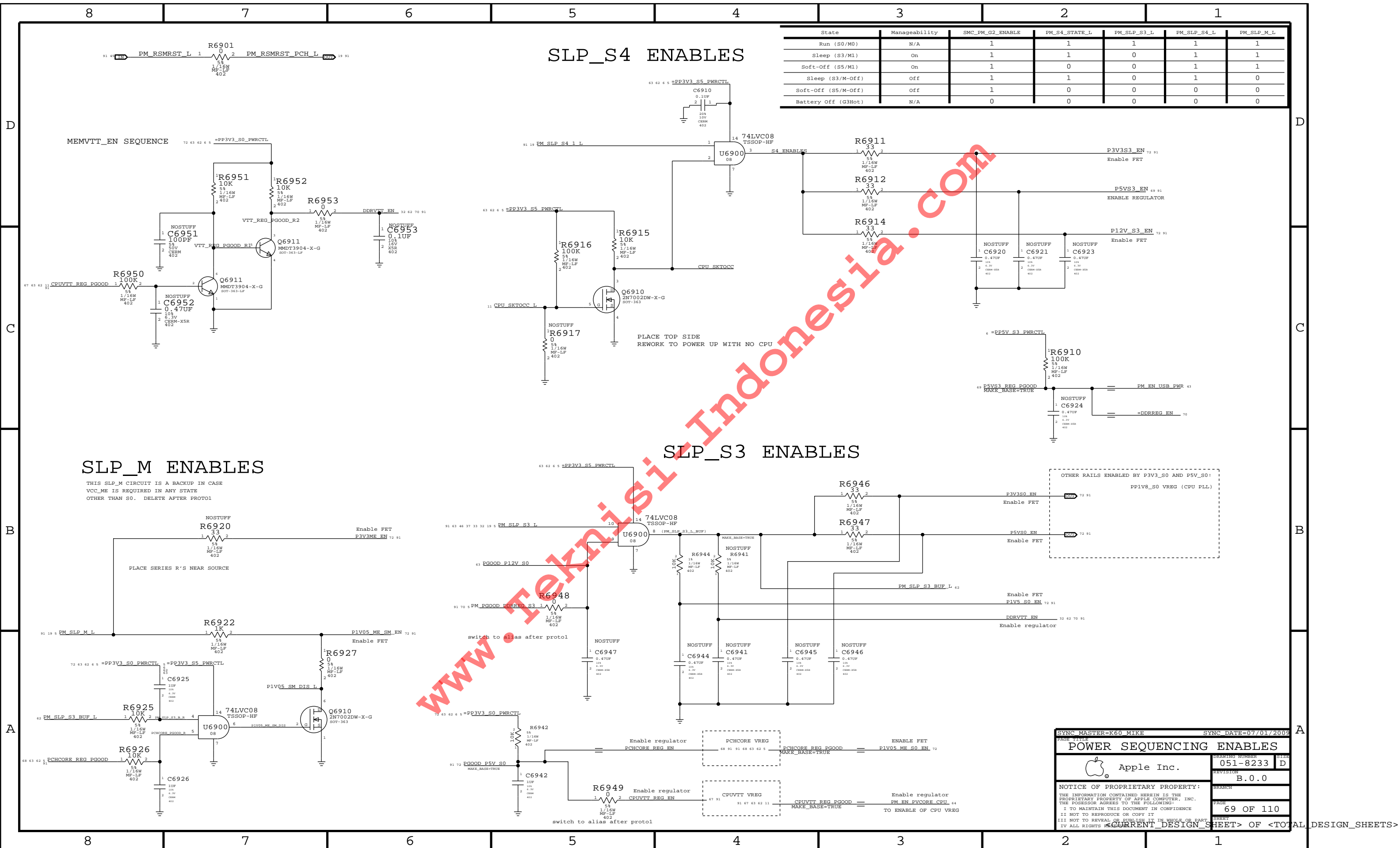


FLP = 8.82 KHZ
FHP = 80 HZ

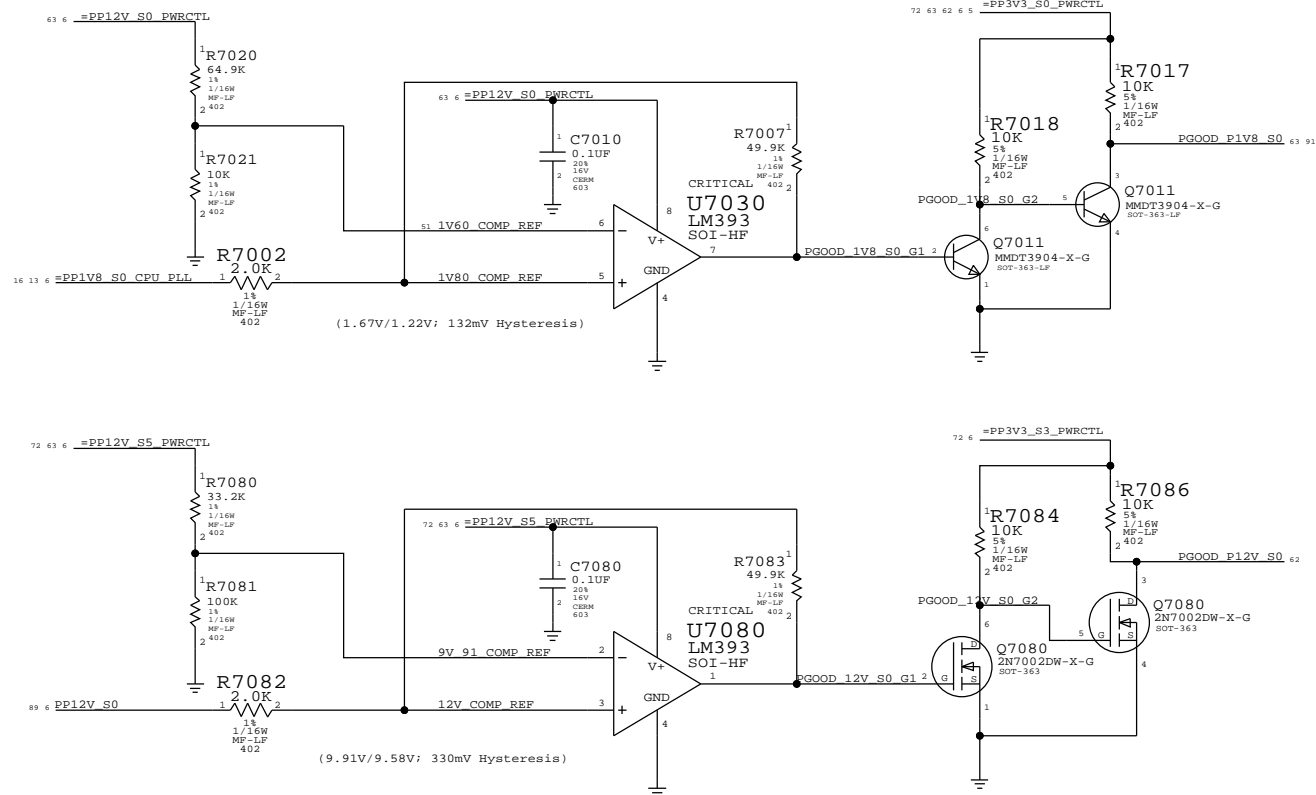


PAGE TITLE		SYNC MASTER=K23 SKIP		SYNC DATE=07/16/2009	
AUDIO: Mikey		DRAWING NUMBER		SIZE	
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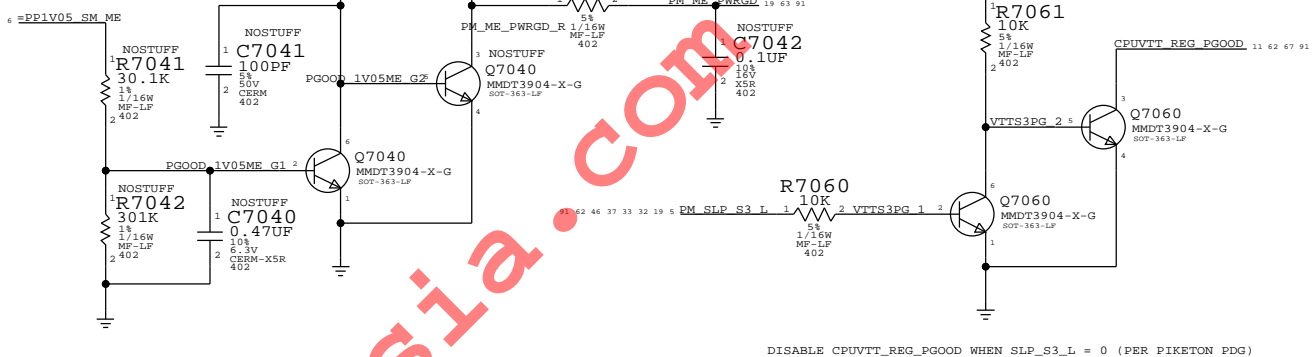


PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0

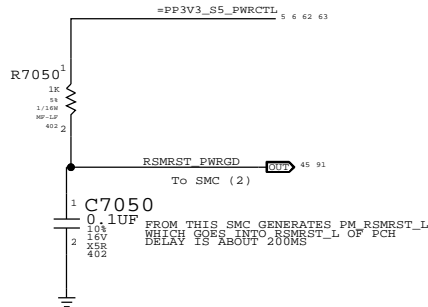


ME PGOOD SEQUENCE

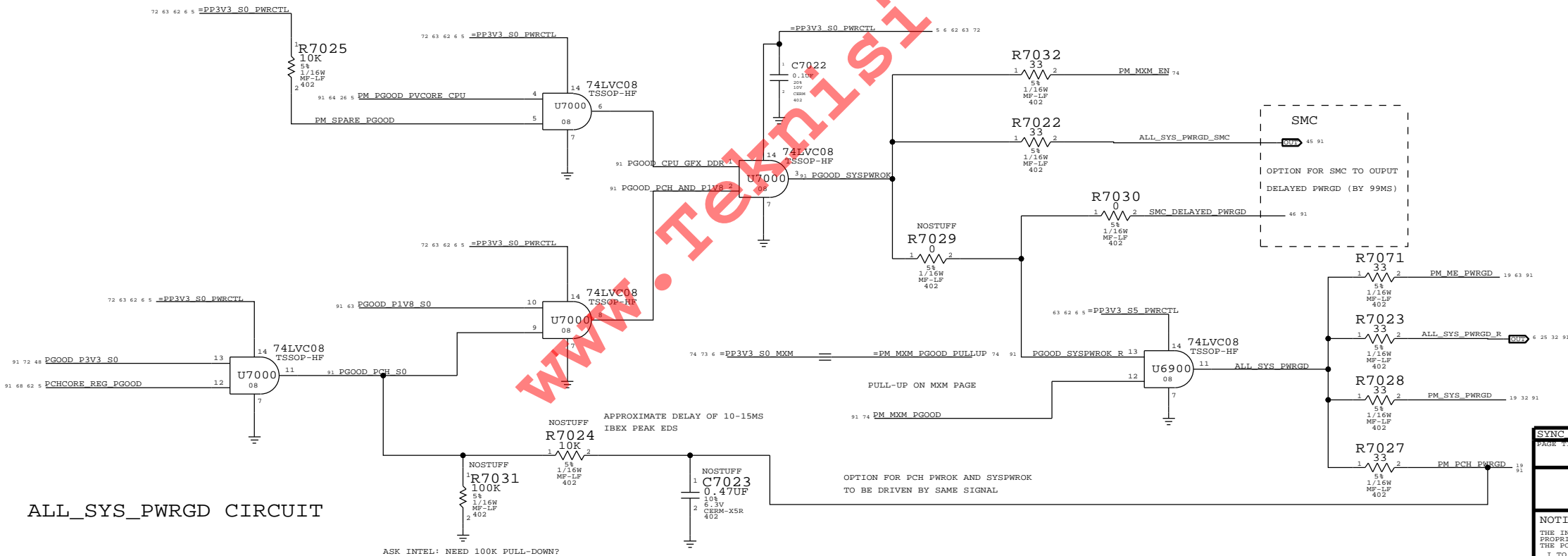
DELAY REQUIREMENTS
8.3 MS ON RISE/ 2.8MS ON FALL
COMPONENT VALUES FROM CRB
NEED TO VERIFY TIMINGS



DISABLE CPUVTT_REG_PGOOD WHEN SLP_S3_L = 0 (PER PIKETON PDG)



S0 RAILS PGOOD

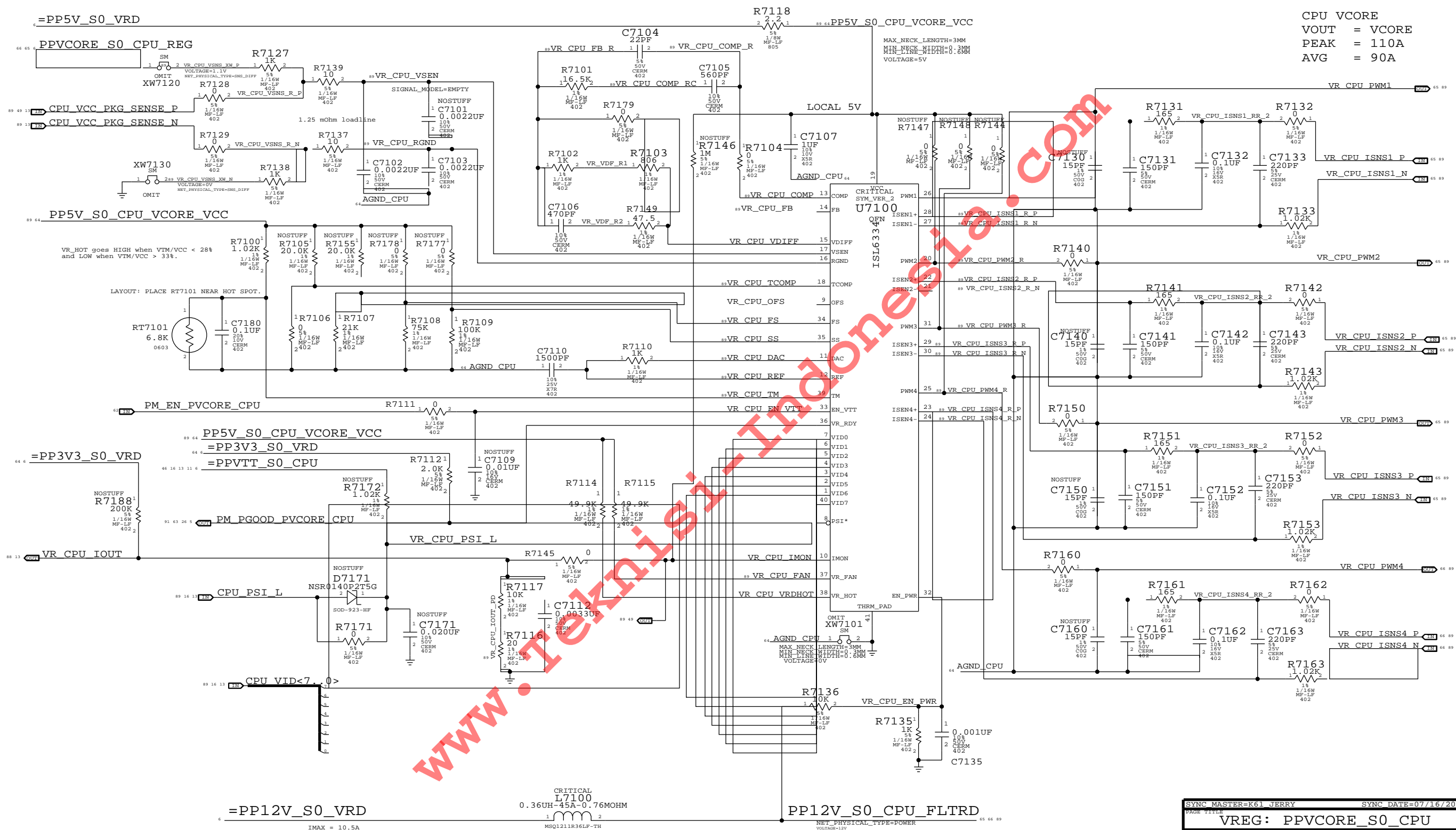


ALL_SYS_PWRGD CIRCUIT

SYNC MASTER=K60 MIKE		SYNC DATE=07/01/2009	
POWER SEQUENCING PGOOD		DRAWING NUMBER 051-8233 D	
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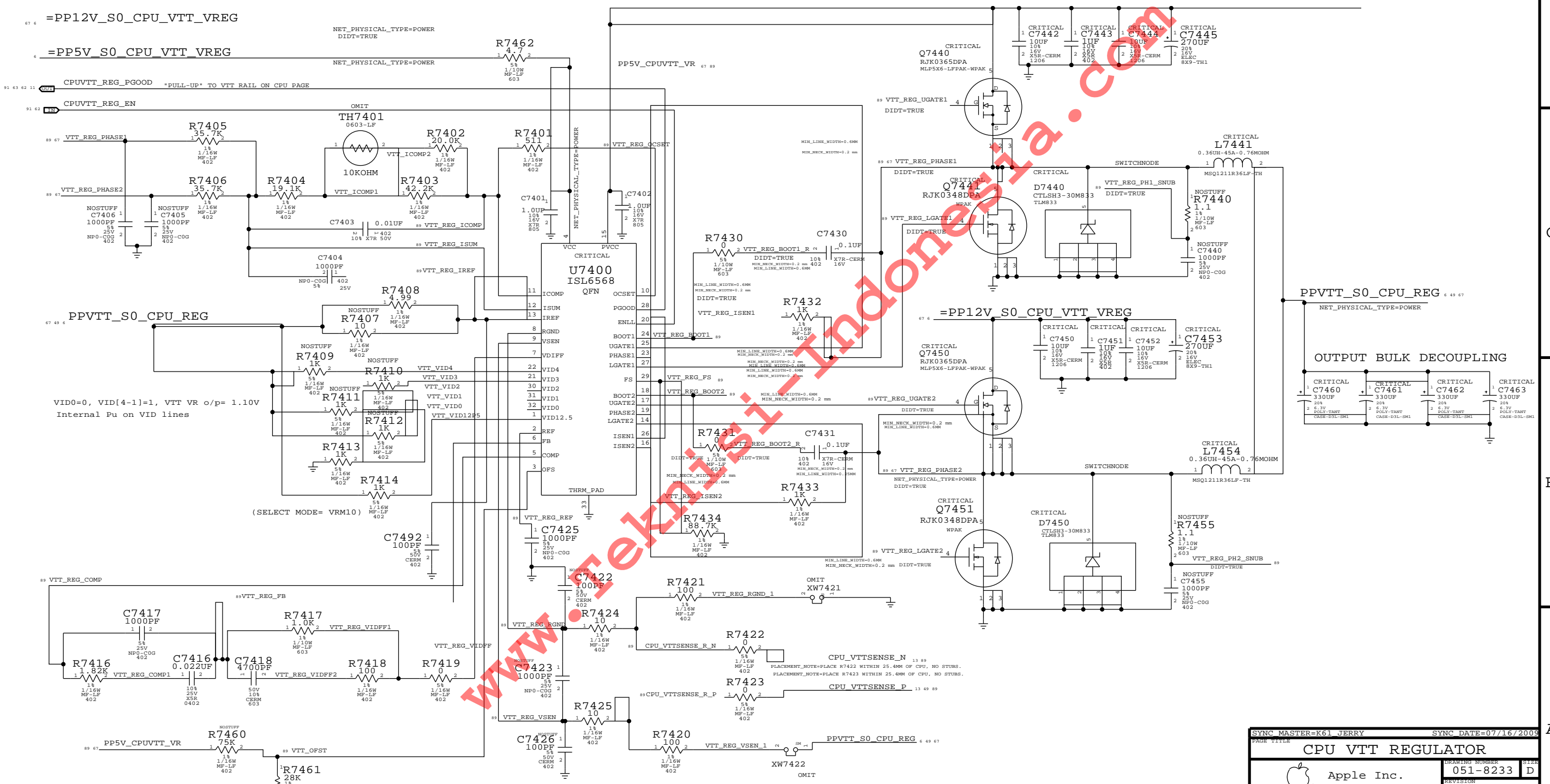
CPU CORE REG 1.1V/110A O/P= PPVCORE_S0_CPU_REG



SYNC MASTER=K61 JERRY		SYNC DATE=07/16/2009	
PAGE TITLE		VREG: PPVCORE_S0_CPU	
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CPU VTT REG 1.1V/30A O/P= PPVTT_S0_CPU_REG

CPU VTT
VOUT = 1.1V OR 1.05V
PEAK = 35A
AVG = 30A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
113S0127	1	RES, 68K, 0603, 5%	TH7401	

SYNC MASTER=K61 JERRY

SYNC DATE=07/16/2009

CPU VTT REGULATOR

Apple Inc.

051-8233

B.0.0

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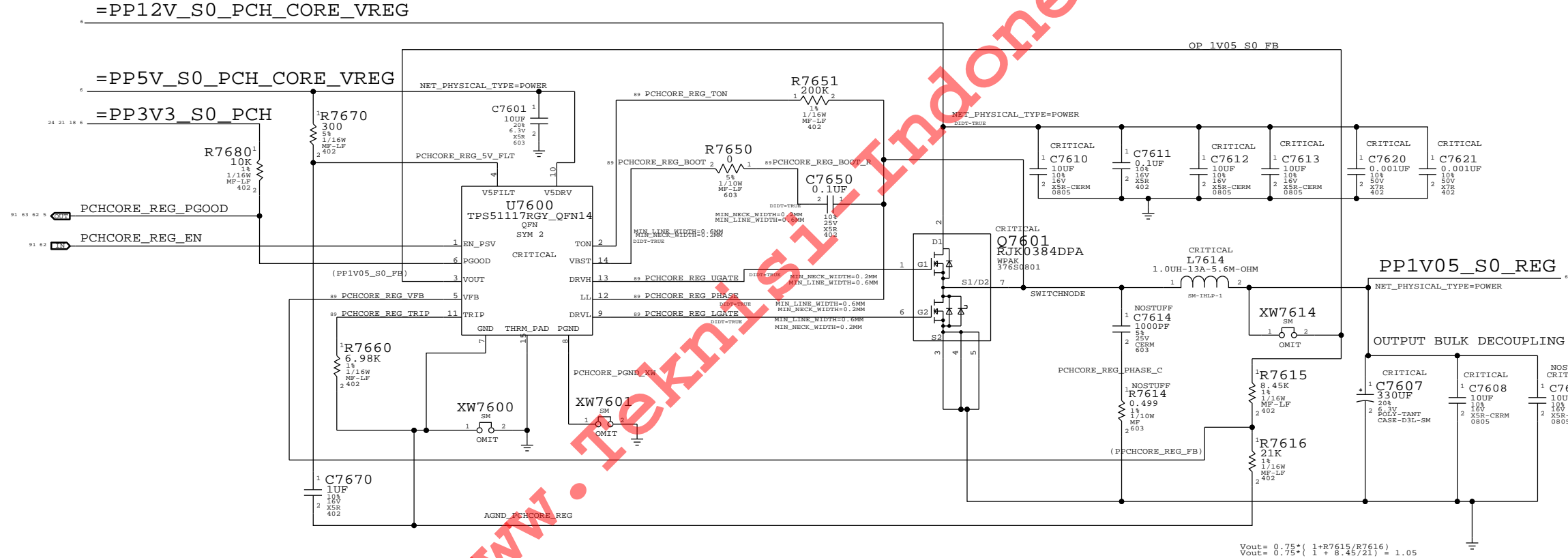
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CURRENT DESIGN SHEET

OF TOTAL DESIGN SHEETS

IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG
VOUT = 1.05V
PEAK = 7.5A
AVG = 3A




[illegible]

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

The schematic diagram illustrates the P1V8 voltage regulator circuit. It is powered by PP5V_S0_P1V8_VREG. The circuit includes several capacitors (C7854, C7855, C7851, C7850, C7852, C7853, and C7854) and resistors (R7852, R7853, R7850, and R7851). The U7850 (ISL8009B) is the central voltage regulator. The output is P1V8_S0_REG. A large red watermark 'www' is overlaid on the diagram.

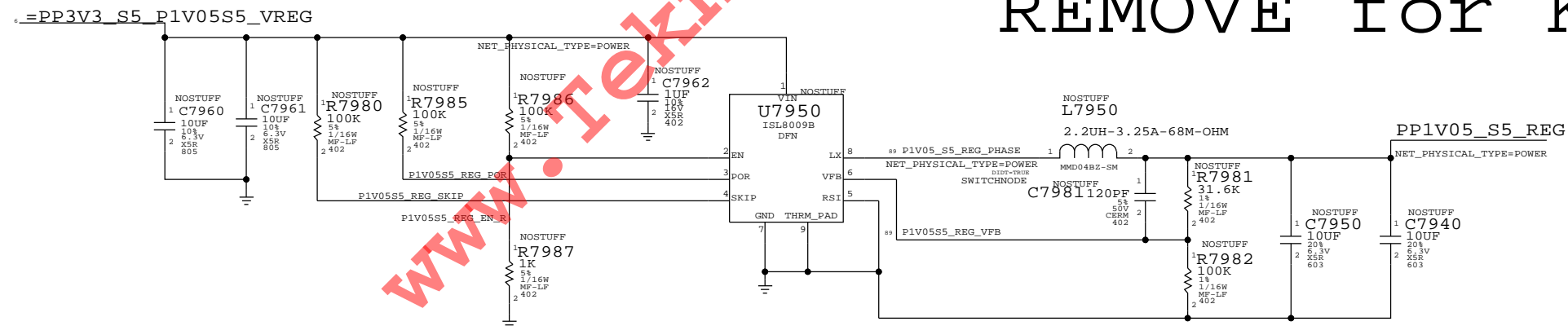
$$V_o = 0.8 * (1 + R_a/R_b)$$
$$V_o = 0.8 * (1 + 59/47) = 1.804V$$


SYNC MASTER-K60 JERRY		SYNC DATE=07/01/2009	
PAGE TITLE			
1.5V / 1.8V VREGS			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8233		D
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	B.0.0		
BRANCH			
PAGE		78 OF 110	
SHEET		OF <TOTAL>	

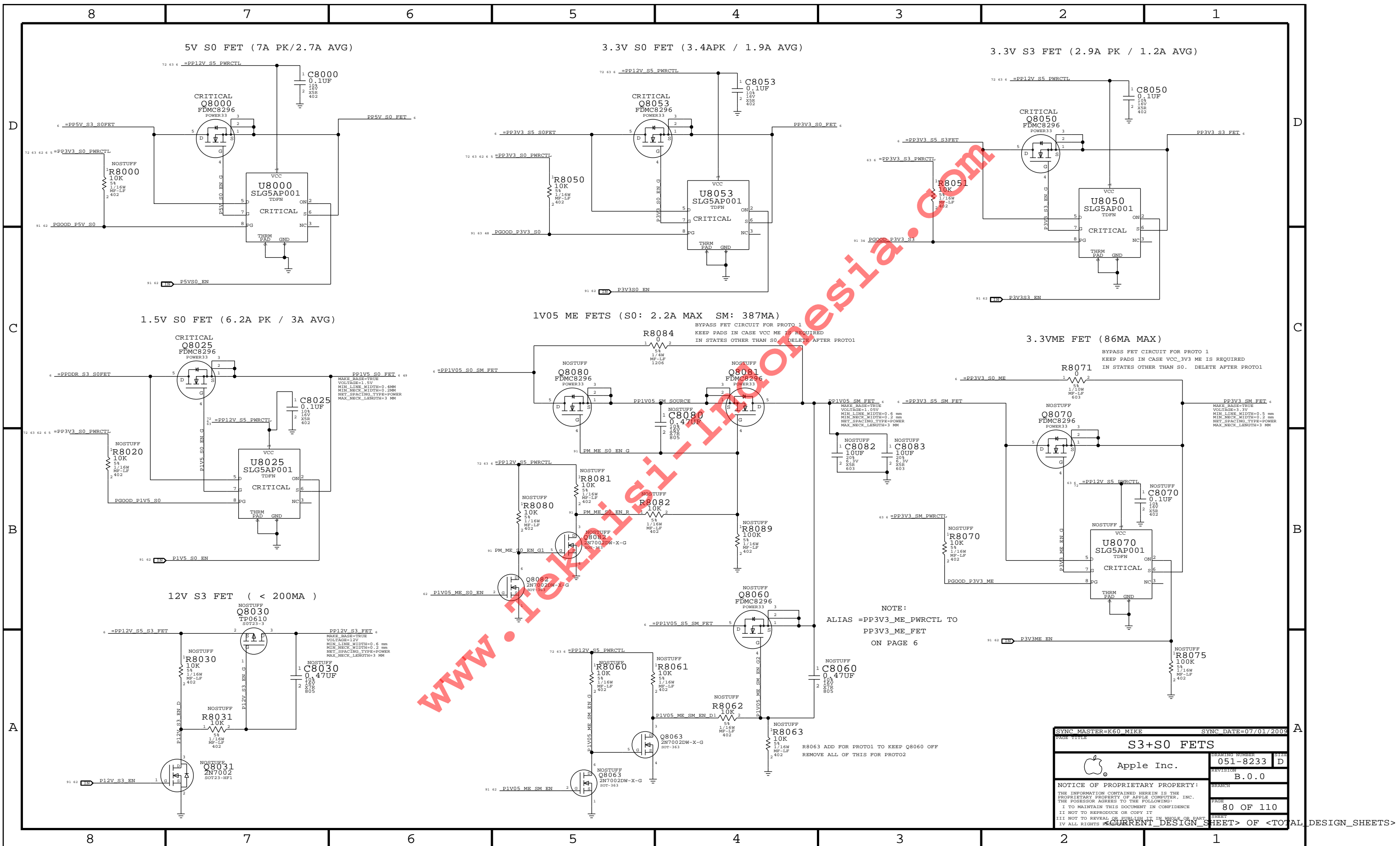
Supply needs to guarantee 3.31V delivered to SMC VRef generator



REMOVE for K60/K61



SYNC MASTER-K60 JERRY		SYNC DATE=07/01/2009	
PAGE TITLE			
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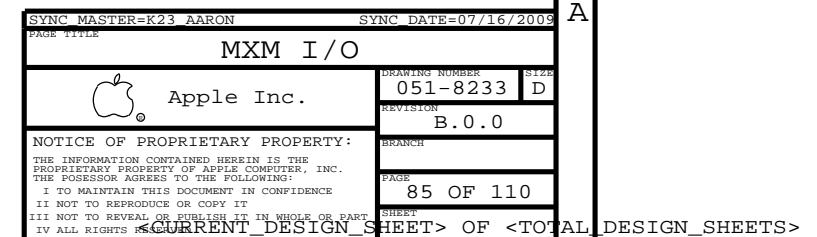
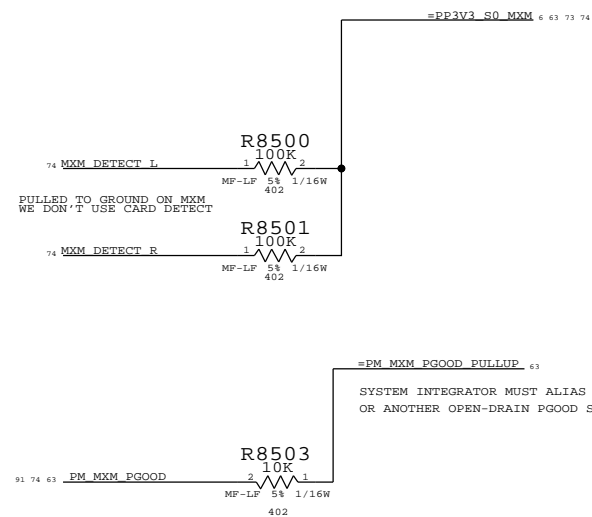
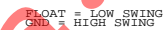
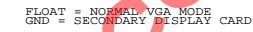
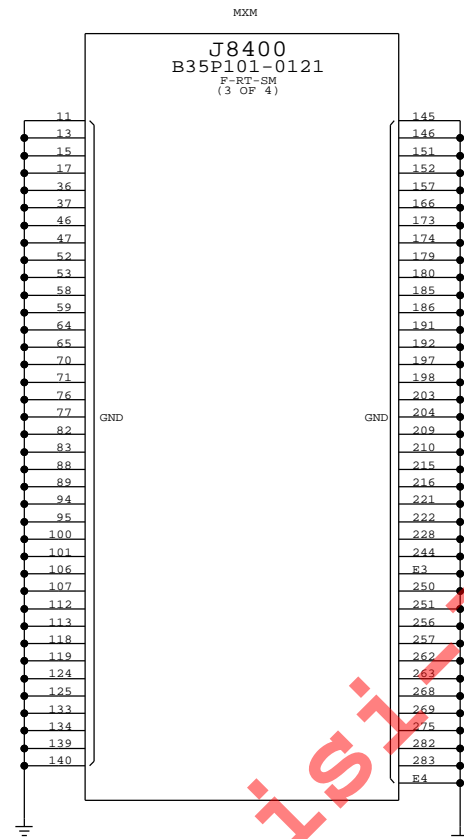
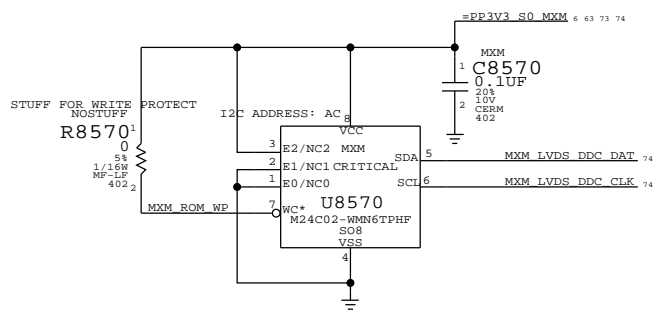
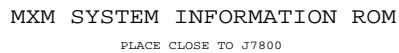
Power aliases required by this page:

- =PP3V3_S0_MXM

Signal aliases required by this page:

- =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:




8	7	6	5	4	3	2	1
MXM TX CAPS				MXM RX CAPS			
84	9	PEG_R2D_C_P<0>	MXM C8600 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	84 73	84
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SYNC MASTER=K60 AARON

SYNC DATE=07/01/2009

PAGE TITLE

MXM PCIE CAPS

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Page Notes

Power aliases required by this page:
- =PF3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Unused MXM Interfaces

Unused MXM DP Interfaces

Display: Aliases

SYNC_MASTER=K61_AARON SYNC_DATE=07/01/2009

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NONE	76	92

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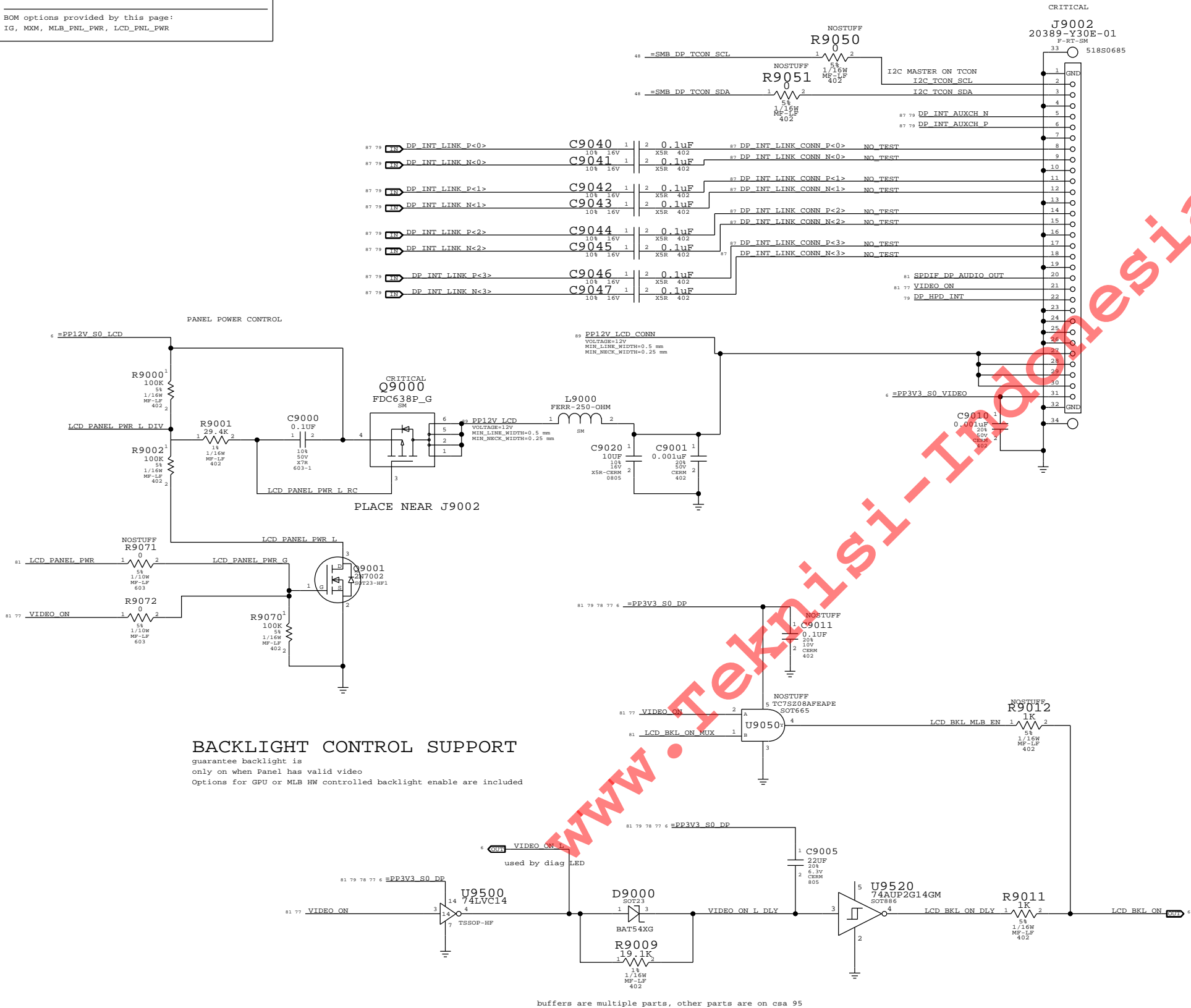
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
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BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

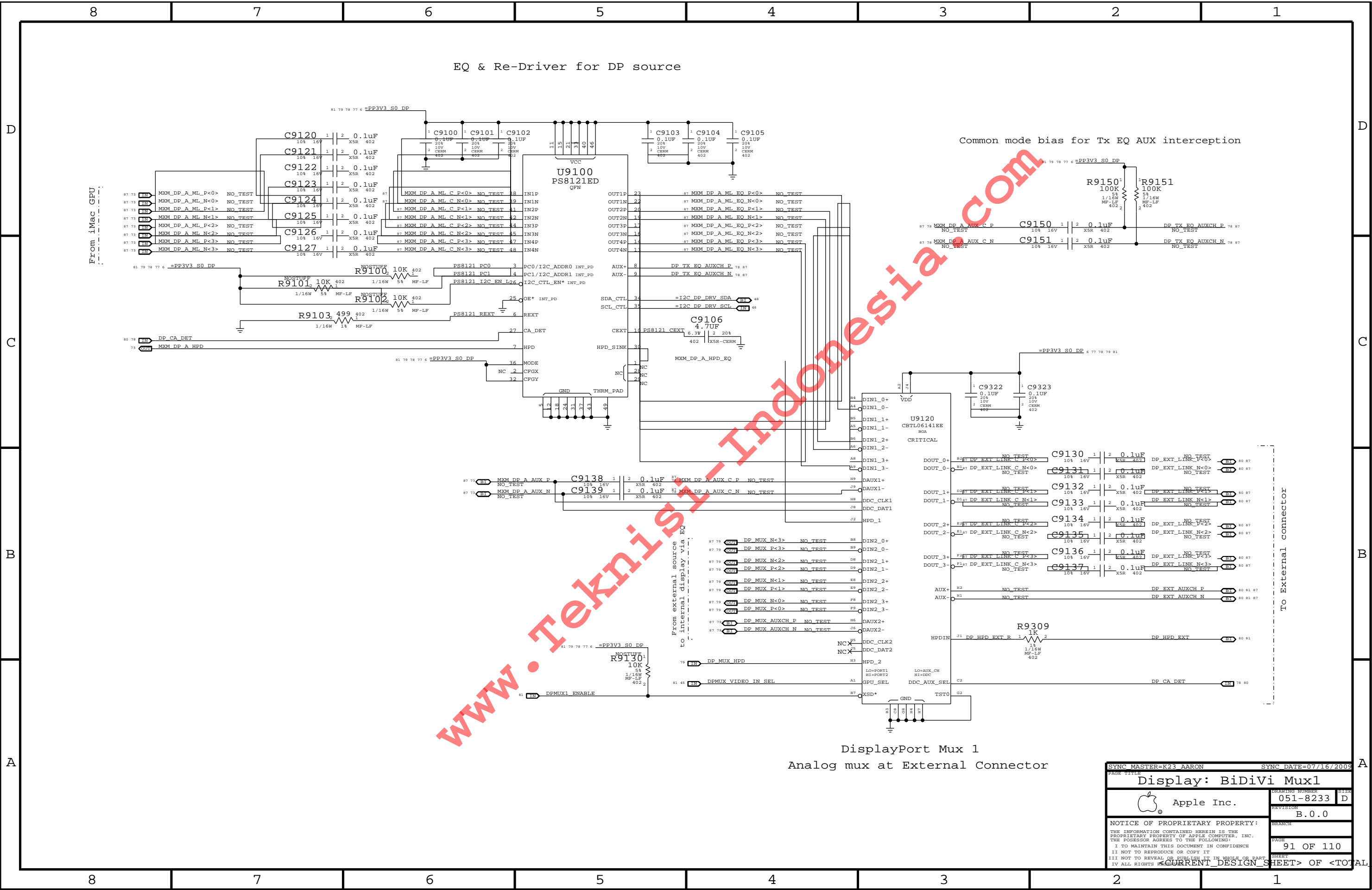



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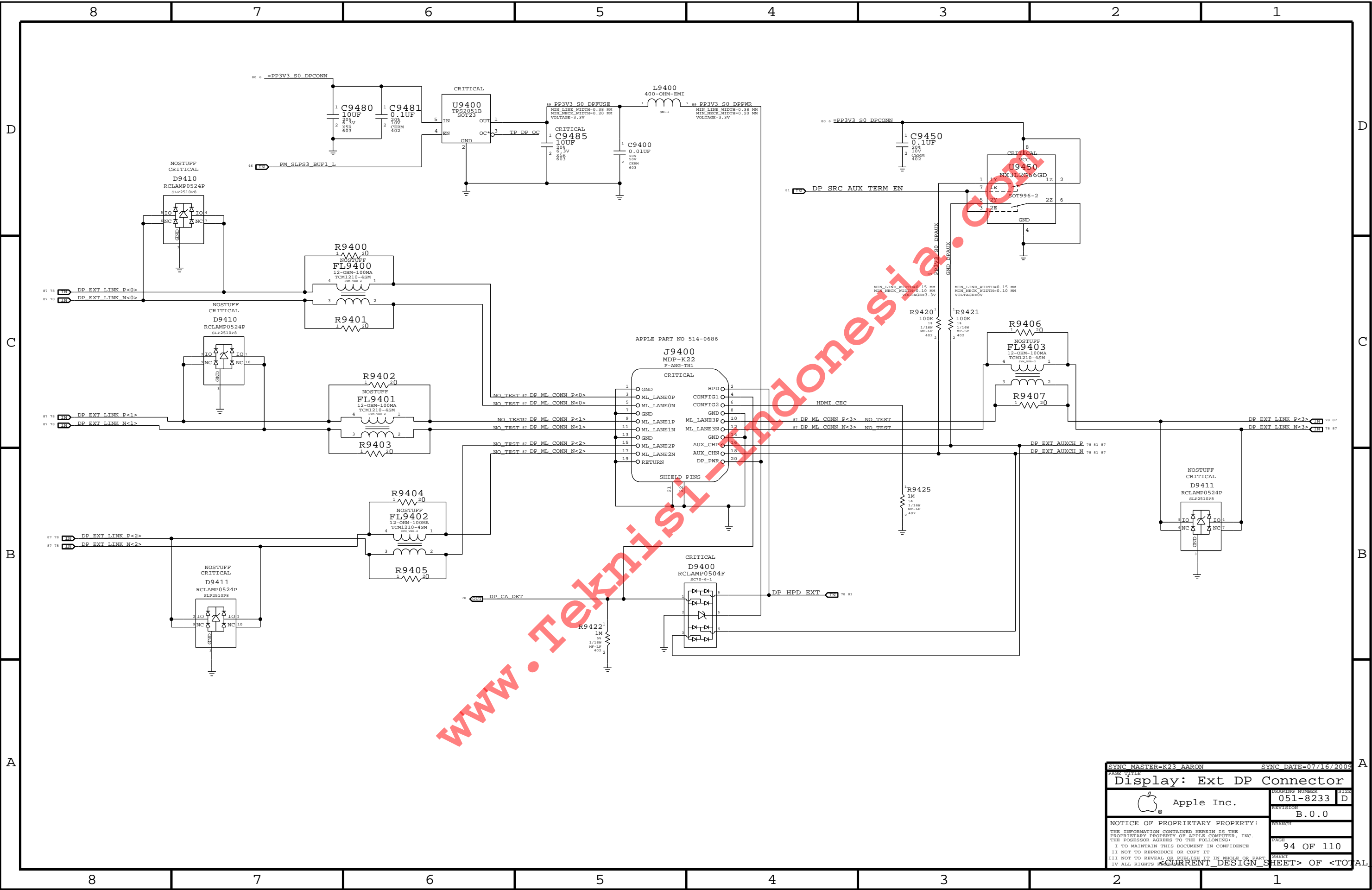
Display: Int DP Connector


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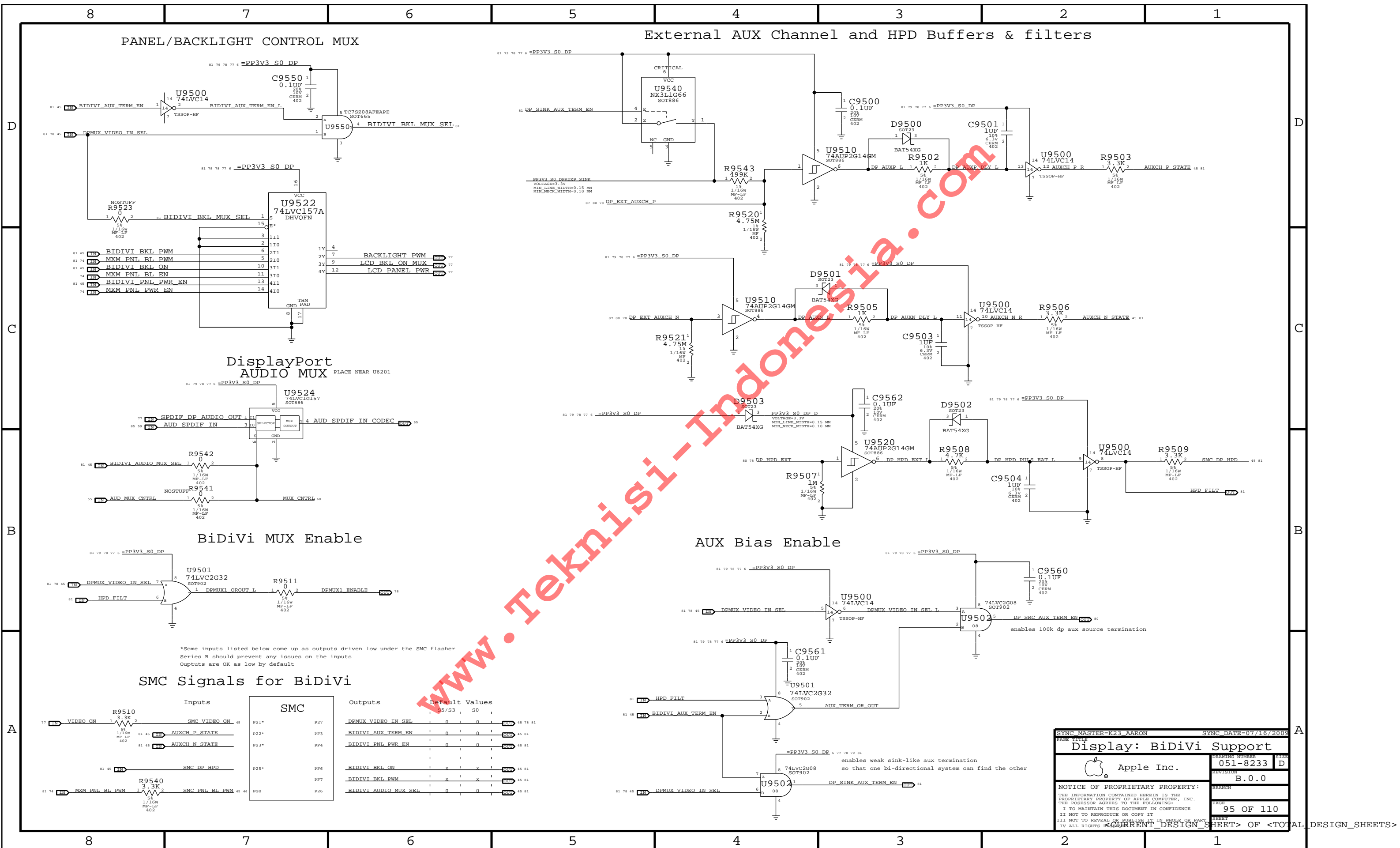


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Display: Ext DP Connector			
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_35S	*	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_ODD2DQ_ODD	*	=3:1_SPACING	?
MEM_DQ_ODD2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_EVEN	*	=3:1_SPACING	?
MEM_DQ_EVEN2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_ODD	*	=5:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20THER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM	MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM	MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM	MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_CLK	MEM_DQ_ODD	*	MEM_CLK2MEM	MEM_DQS	MEM_DQ_ODD	*	MEM_DQS2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM	MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_CLK	MEM_DQ_EVEN	*	MEM_CLK2MEM	MEM_DQS	MEM_DQ_EVEN	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_ODD	MEM_CLK	*	MEM_DQ_ODD2MEM	MEM_DQ_EVEN	MEM_CLK	*	MEM_DQ_EVEN2MEM
MEM_DQ_ODD	MEM_CTRL	*	MEM_DQ_ODD2MEM	MEM_DQ_EVEN	MEM_CTRL	*	MEM_DQ_EVEN2MEM
MEM_DQ_ODD	MEM_CMD	*	MEM_DQ_ODD2MEM	MEM_DQ_EVEN	MEM_CMD	*	MEM_DQ_EVEN2MEM
MEM_DQ_ODD	MEM_DQ_ODD	*	MEM_DQ_ODD2DQ_ODD	MEM_DQ_EVEN	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_EVEN
MEM_DQ_ODD	MEM_DQS	*	MEM_DQ_ODD2MEM	MEM_DQ_EVEN	MEM_DQS	*	MEM_DQ_EVEN2MEM
MEM_DQ_ODD	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_ODD	MEM_DQ_EVEN	MEM_DQ_ODD	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_ODD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_EVEN	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20THER
MEM_CTRL	*	*	MEM_20THER
MEM_CMD	*	*	MEM_20THER
MEM_DQ_ODD	*	*	MEM_20THER
MEM_DQS	*	*	MEM_20THER
MEM_DQ_EVEN	*	*	MEM_20THER

Need to support MEM_*-style wildcards!

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER_PHY	*	MEM_POWER_WIDTH	MEM_POWER	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_RCOMP_PHY	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD
























SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_RCOMP	*	0.2 MM	?

Memory Net Properties


MEMORY POWER PROPERTIES

		NET_TYPE		
VOLTAGE	PHYSICAL	SPACING		
REF0	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A	12 28
REF0	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B	12 28
REF0	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMM_A_DQ	28
REF0	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMM_B_DQ	28
REF0	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A_SW	28
REF0	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B_SW	28

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
	PHYSICAL	SPACING		
	MEM_750p	MEM_DQS	MEM_B_DQS_P<0>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_N<0>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_P<1>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_N<1>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_P<2>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_N<2>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_P<3>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_N<3>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_P<4>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_N<4>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_P<5>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_N<5>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_P<6>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_N<6>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_P<7>	12 32
	MEM_750p	MEM_DQS	MEM_B_DQS_N<7>	12 32
	MEM_RCOMP_DRV	MEM_RCOMP	CPU_SM_RCOMP0	11
	MEM_RCOMP_DRV	MEM_RCOMP	CPU_SM_RCOMP1	11
	MEM_RCOMP_DRV	MEM_RCOMP	CPU_SM_RCOMP2	11
	MEM_750p	MEM_DQS	TP MEM_B_DQS_P<8>	8 12
	MEM_750p	MEM_DQS	TP MEM_B_DQS_N<8>	8 12
	MEM_750p	MEM_DQS	TP MEM_A_DQS_P<8>	8 12
	MEM_750p	MEM_DQS	TP MEM_A_DQS_N<8>	8 12

```
ADD RULES TO NC_DQS<8>
TO CLEAR CHECK_PLUS ERRORS
```

SYNCH MASTER-K60 MIKE		SYNCH DATE=07/01/2009	
DRAWN TITLE			
Memory Constraints			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8233		D
		REVISION	
		B.0.0	
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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
KNET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BUF0_CLK	*	= 3:1_SPACING	?
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE: BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?

SOURCE: BROADCOM 5764-DS04-RDS. PAGE 38

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		SPACING	
		PHYSICAL			
		ENET_50S	ENET_5S	ENET_RDAC	36
		ENET_50S	BUFF_CLK	ENET_CLK25M_XTALI	36
		ENET_50S	BUFF_CLK	ENET_CLK25M_XTALO	36
		ENET_50S	BUFF_CLK	ENET_CLK25M_XTAL	36
		ENET_100S	ENET_DIFP	ENET MDI P<3..0>	36 38
		ENET_100S	ENET_DIFP	ENET MDI N<3..0>	36 38
		ENET_100S	ENET_DIFP	ENET MDI T P<3..0>	36
		ENET_100S	ENET_DIFP	ENET MDI T N<3..0>	36
		ENET_100S	ENET_MII	PCIE ENET R2D P	36
		ENET_100S	ENET_MII	PCIE ENET R2D N	36
		ENET_100S	ENET_MII	PCIE ENET D2R P	36 38
		ENET_100S	ENET_MII	PCIE ENET D2R N	36 38
		ENET_100S	ENET_MII	PCIE ENET R2D C P	36 38
		ENET_100S	ENET_MII	PCIE ENET R2D C N	36 38
		ENET_100S	ENET_MII	PCIE ENET D2R C P	36
		ENET_100S	ENET_MII	PCIE ENET D2R C N	36

FireWire Interface Constraints

[illegible]















SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?


FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_PHY	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=STANDARD	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT.NET		NET_TYPE		
		PHYSICAL	SPACING	
		FW_110G	FW_TP	FW_PORT0_TPA_P 40 41
		FW_110G	FW_TP	FW_PORT0_TPA_N 40 41
		FW_110G	FW_TP	FW_PORT0_TPB_P 40 41
		FW_110G	FW_TP	FW_PORT0_TPB_N 40 41
PORT 1 & 2 NOT USED				
		FW_110G	FW_TP	FW_P0_TPA_L_P 40
		FW_110G	FW_TP	FW_P0_TPA_L_N 40
		FW_110G	FW_TP	FW_P0_TPB_L_P 40
		FW_110G	FW_TP	FW_P0_TPB_L_N 40
UNUSED FW NETS PHYSICAL PROPERTIES				
		FW_110G	FW_TP	FW_P1_TPA_P 39 40
		FW_110G	FW_TP	FW_P1_TPA_N 39 40
		FW_110G	FW_TP	FW_P2_TPA_P 39 40
		FW_110G	FW_TP	FW_P2_TPA_N 39 40
AUDIO MIC PHYSICAL PROPERTIES				
	AUDIO_PHY	AUDIO	AUD_MIC1_IN_N	59 60
	AUDIO_PHY	AUDIO	AUD_MIC1_IN_P	59 60


SYMC MASTER-K60 AARON		SYMC DATE=07/01/2009	
PAGE TITLE			
ENET/FIREWIRE CONSTRAINTS			
 Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		B.0.0	
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DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF																																																																																																																																																																																																																																																																																																	
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MGR.</td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP ML CONN P<3..0></td><td>80</td></tr><tr><td>DP_85D</td><td>DISPLAYPORT</td><td>DP ML CONN N<3..0></td><td>80</td></tr><tr><td>DP_85D</td><td>DISPLAYPORT</td><td>DP INT LINK CONN P<3..0></td><td>77</td></tr><tr><td>DP_85D</td><td>DISPLAYPORT</td><td>DP INT LINK CONN N<3..0></td><td>77</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP INT LINK P<3..0></td><td>77 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP INT LINK N<3..0></td><td>77 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP INT AUXCH P</td><td>77 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP INT AUXCH N</td><td>77 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP EXT LINK P<3..0></td><td>77 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP EXT LINK N<3..0></td><td>78 80</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP EXT AUXCH P</td><td>78 80</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP EXT AUXCH N</td><td>78 80 81</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP EXT LINK C P<3..0></td><td>78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP EXT LINK C N<3..0></td><td>78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP A ML P<3..0></td><td>73 78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP A ML N<3..0></td><td>73 78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP A AUX C P</td><td>78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP A AUX C N</td><td>78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP A AUX P</td><td>73 78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP A AUX N</td><td>73 78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP C ML P<3..0></td><td>73 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP C ML N<3..0></td><td>73 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP C AUX P</td><td>73 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP C AUX N</td><td>73 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP C AUX C P</td><td>79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP C AUX C N</td><td>79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP MUX P<3..0></td><td>78 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP MUX N<3..0></td><td>78 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP MUX AUXCH P</td><td>78 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP MUX AUXCH N</td><td>78 79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP EQLZ AUXCH P</td><td>79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP EQLZ AUXCH N</td><td>79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP A ML C P<3..0></td><td>78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP A ML C N<3..0></td><td>78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP C ML C P<3..0></td><td>79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP C ML C N<3..0></td><td>79</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP TX EQ AUXCH P</td><td>78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>DP TX EQ AUXCH N</td><td>78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP A ML EQ P<3..0></td><td>78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP A ML EQ N<3..0></td><td>78</td></tr><tr><td colspan="5">UNUSED VIDEO NET PHYSICAL CONSTRAINTS</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP B AUX P</td><td>73 78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP B AUX N</td><td>73 78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP D AUX P</td><td>73 78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP D AUX N</td><td>73 78</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM LVDS A CLK P</td><td>74 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM LVDS A CLK N</td><td>74 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM LVDS B CLK P</td><td>74 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM LVDS B CLK N</td><td>74 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP B ML P<3..0></td><td>73 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP B ML N<3..0></td><td>73 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP D ML P<3..0></td><td>73 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM DP D ML N<3..0></td><td>73 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM LVDS A DATA P<3..0></td><td>74 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM LVDS A DATA N<3..0></td><td>74 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM LVDS B DATA P<3..0></td><td>74 76</td></tr><tr><td></td><td>DP_85D</td><td>DISPLAYPORT</td><td>MXM LVDS B DATA N<3..0></td><td>74 76</td></tr></table>								ELECTRICAL_CONSTRAINT_SET	NET_TYPE				PHYSICAL	SPACING	ASSIGNED IN CONT. MGR.	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GRAPHICS CONSTRAINTS

 Apple Inc.

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<div><div>SMBus Interface Constraints</div><table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>SMB_55S</td><td>*</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr></table><div><table><tr><th>SPACING_RULE_SET</th><th>LAYER</th><th>LINE-TO-LINE SPACING</th><th>WEIGHT</th></tr><tr><td>SMB</td><td>*</td><td>=2x_DIELECTRIC</td><td>?</td></tr></table><table><tr><th>NET_SPACING_TYPE1</th><th>NET_SPACING_TYPE2</th><th>AREA_TYPE</th><th>SPACING_RULE_SET</th></tr><tr><td>THERMAL</td><td>*</td><td>*</td><td>4:1_SPACING</td></tr><tr><td>THERMAL</td><td>POWER</td><td>*</td><td>PWR_P2MM</td></tr><tr><td>THERMAL</td><td>GND</td><td>*</td><td>GND_P2MM</td></tr></table><table><tr><th>NET_PHYSICAL_TYPE</th><th>AREA_TYPE</th><th>PHYSICAL_RULE_SET</th></tr><tr><td>THERM_DIFF</td><td>*</td><td>1:1_DIFFPAIR</td></tr><tr><td>SNS_DIFF</td><td>*</td><td>1:1_DIFFPAIR</td></tr></table></div></div>								PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SMB	*	=2x_DIELECTRIC	?	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	THERMAL	*	*	4:1_SPACING	THERMAL	POWER	*	PWR_P2MM	THERMAL	GND	*	GND_P2MM	NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	THERM_DIFF	*	1:1_DIFFPAIR	SNS_DIFF	*	1:1_DIFFPAIR																																																																																																																																																																																																																			
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5V	PP5V S3 HDR REG V5P10	
5V	PP5V S3 CAMERA FIT	43
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5V	VREFMARGIN DIMMA P5V	28
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5V		
5V	PP5V S5	6
5V	PP5V S5 PCH VREFSUPS	22 24
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5V	PP5V USB2 PORT0	43
5V	PP5V USB2 PORT0 F	43
5V	PP5V USB2 PORT1	43
5V	PP5V USB2 PORT1 F	43
5V	PP5V USB2 PORT2	43
5V	PP5V USB2 PORT2 F	43
5V	PP5V USB2 PORT3	43
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
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	FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT									
D	J4700 USB CAMERA									D
	<div><div>85 44</div><div>PP5V_S3_CAMERA</div><div>FUNC_TEST=TRUE</div><div>RIN_ALLOWED_TPS=1</div></div> <div><div>85 44</div><div>USB_CAMERA_L_P</div><div>FUNC_TEST=TRUE</div></div> <div><div>85 44</div><div>USB_CAMERA_L_N</div><div>FUNC_TEST=TRUE</div></div> <div>1 PP5V_S3_REG Testpoint near J4700</div> <div>2 Ground Testpoints near J4700</div>									
	J4750 USB CARD READER									
	<div><div>85 44</div><div>USB_SDCARD_L_P</div><div>FUNC_TEST=TRUE</div></div> <div><div>85 44</div><div>USB_SDCARD_L_N</div><div>FUNC_TEST=TRUE</div></div> <div><div>91 44 25 21</div><div>SDCARD_RESET</div><div>FUNC_TEST=TRUE</div></div> <div>1 PP3V3_S3 Testpoint near J4750</div> <div>2 Ground Testpoints near J4750</div>									
C	J4720 USB BLUETOOTH									C
	<div><div>85 44</div><div>USB_BT_L_P</div><div>FUNC_TEST=TRUE</div></div> <div><div>85 44</div><div>USB_BT_L_N</div><div>FUNC_TEST=TRUE</div></div> <div>1 PP3V3_S3 Testpoint near J4720</div> <div>2 Ground Testpoints near J4720</div>									
	J4780 IR BOARD									
	<div><div>85 44</div><div>USB_IR_L_P</div><div>FUNC_TEST=TRUE</div></div> <div><div>85 44</div><div>USB_IR_L_N</div><div>FUNC_TEST=TRUE</div></div> <div>1 PP5V_S3_REG Testpoint near J4780</div> <div>2 Ground Testpoints near J4780</div>									
B	J4520 SATA ODD (HIGH SPEED)									B
	<div><div>84 43</div><div>SATA_ODD_R2D_P</div><div>FUNC_TEST=TRUE</div></div> <div><div>84 43</div><div>SATA_ODD_R2D_N</div><div>FUNC_TEST=TRUE</div></div> <div><div>84 43</div><div>SATA_ODD_D2R_C_N</div><div>FUNC_TEST=TRUE</div></div> <div><div>84 43</div><div>SATA_ODD_D2R_C_P</div><div>FUNC_TEST=TRUE</div></div> <div><div>45 43</div><div>SMC_ODD_DETECT</div><div>FUNC_TEST=TRUE</div></div> <div>1 PP5V_S0 Testpoint near J4520</div> <div>5 Ground Testpoints near J4520</div>									
	J4510 SATA HDD (HIGH SPEED)									
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A	J5520 ANALOG LCD TEMP SENSOR									A
	<div><div>88 51</div><div>SNS_LCD_P</div><div>FUNC_TEST=TRUE</div></div> <div><div>88 51</div><div>SNS_LCD_N</div><div>FUNC_TEST=TRUE</div></div>									
	J5521 AMBIENT TEMP SENSOR									
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	J5551 ODD TEMP SENSOR									
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	J5700 CPU FAN									
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	J5601 HD FAN									
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	J5550 HDD TEMP SENSOR									
	<div><div>88 51</div><div>HDD_OOB_TEMP_FILT</div><div>FUNC_TEST=TRUE</div></div>									
	J5560 SKIN TEMP SENSOR									
	<div><div>88 51</div><div>SNS_SKIN_P</div><div>FUNC_TEST=TRUE</div></div> <div><div>88 51</div><div>SNS_SKIN_N</div><div>FUNC_TEST=TRUE</div></div>									
	J6601 AUDIO MICROPHONE									
	<div><div>59</div><div>AUD_MIC_IN1_N_CONN</div><div>FUNC_TEST=TRUE</div></div> <div><div>59</div><div>GND_AUDIO_MIC1_CONN</div><div>FUNC_TEST=TRUE</div></div> <div><div>59</div><div>AUD_MIC_IN1_P_CONN</div><div>FUNC_TEST=TRUE</div></div> <div>1 Ground Testpoint near J6601</div>									
	J6602 AUDIO RIGHT SPEAKER									
	<div><div>85 59 58</div><div>AUD_SPKR_OUTLO2R_POUT</div><div>FUNC_TEST=TRUE</div></div> <div><div>85 59 58</div><div>AUD_SPKR_OUTLO2R_NOUT</div><div>FUNC_TEST=TRUE</div></div> <div><div>85 59 57</div><div>AUD_SPKR_OUTLO1R_POUT</div><div>FUNC_TEST=TRUE</div></div> <div><div>85 59 57</div><div>AUD_SPKR_OUTLO1R_NOUT</div><div>FUNC_TEST=TRUE</div></div>									
	J6603 AUDIO LEFT SPEAKER									
	<div><div>85 59 58</div><div>AUD_SPKR_OUTLO2L_POUT</div><div>FUNC_TEST=TRUE</div></div> <div><div>85 59 58</div><div>AUD_SPKR_OUTLO2L_NOUT</div><div>FUNC_TEST=TRUE</div></div> <div><div>85 59 57</div><div>AUD_SPKR_OUTLO1L_POUT</div><div>FUNC_TEST=TRUE</div></div> <div><div>85 59 57</div><div>AUD_SPKR_OUTLO1L_NOUT</div><div>FUNC_TEST=TRUE</div></div>									
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